

# ON LINE PROTECTION OF TRANSMISSION LINES USING MICROPROCESSOR

By

V. P. SUNNAK

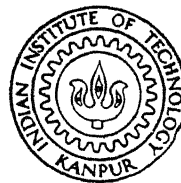
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DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

JULY, 1983

# ON LINE PROTECTION OF TRANSMISSION LINES USING MICROPROCESSOR

A Thesis Submitted  
in Partial Fulfilment of the Requirements  
for the Degree of  
MASTER OF TECHNOLOGY

By  
V. P. SUNNAK

*to the*

DEPARTMENT OF ELECTRICAL ENGINEERING  
INDIAN INSTITUTE OF TECHNOLOGY KANPUR  
JULY, 1983

1980

Dedicated to

my mother

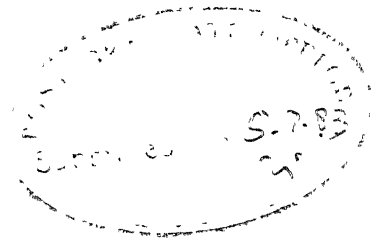
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CERTIFICATE



Certified that this work 'ON LINE PROTECTION OF TRANSMISSION LINE USING MICROPROCESSOR' by V.P. Sunnak has been carried out under my supervision and has not been submitted elsewhere for a degree.

A handwritten signature in dark ink, appearing to be "L.P. Singh", written over a grid of dashed lines.

July 4, 1983

( L.P. Singh )  
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V.P. SUNNAK

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## ABSTRACT

With the increase in complexity of power system network; the need for fast, efficient and reliable protection system has become a necessity. Protection schemes using electromechanical relays has numerous disadvantages and hence they were replaced in the beginning by electronic relays, then by solid state relays. Although these solid state relays are successful in operation, they have certain distinct disadvantages such as time of operation of relay is approximately 3-4 cycles, lack of flexibility and absence of self checking etc. These disadvantages have resulted in a trend towards the use of programmable equipment in place of hardwired systems.

The high speed clearance of fault on the complex power system network, very effectively improves the transient stability limit. The rotational kinetic energy introduced into a power system during a fault is proportional to the square of the fault clearance time. Therefore high speed clearance of faults close to large sources of generation will reduce the system acceleration more than any other form of dynamic control. The fault clearance time depend on the speed of protective relay as well as that of the associated

circuit breaker, the realisation of high speed protective relaying scheme has become imperative.

In this thesis, a review of various method using digital protection algorithms and design and development of microprocessor based on line protective relaying schemes for EHV/UHV transmission lines are outlined.

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## LIST OF PRINCIPAL SYMBOLS

$V_{pk}$	: Peak voltage
$I_{pk}$	: Peak current
$\omega_1$	: normal power frequency of 50 hertz
$\omega_2$	: angular frequency corresponding to data window
$V_d$	: direct axis component of voltage
$V_g$	: quadrature axis component of voltage
$I_d$	: direct axis component of current
$I_q$	: quadrature axis component of current
A/D	: Analogue to digital converter
S/H	: Sample and Hold circuit
CPU	: Central Processing unit
ROM	: Read only memory
RAM	: Random access memory
EPROM	: Evaseable programmable read only memory

# CHAPTER 1

## INTRODUCTION

### 1.1 MOTIVATION

For the protection of EHV/UHV transmission line, a fast, sensitive, reliable, efficient and low cost protection scheme is necessary. The sensitivity and selectivity of a protective scheme depends upon the type of the relay unit employed. Of the several electromagnetic measuring units available, the induction cup unit proved to be the best in distance relaying applications because of its faster speed (3-5 cycles) and greater sensitivity compared to the other types of electromechanical relays and also its ability to produce any type of conventional threshold characteristics.

However, with the advent of solid state devices, such as semiconductor diodes and transistors, a trend towards employing them for relaying purposes, has emerged. The need for faster measuring unit gave impetus to the development of solid state (i.e. static) relays in the initial stages.

The merits of static relays are greater sensitivity, higher speed, lower (VA) burden, no contact problems and immunity from vibrations and shocks etc. due to external causes. The static relays are being used increasingly in recent years, specifically for the protection of EHV/UHV

transmission lines where increased sensitivity, reliability and speed are of importance.

The selectivity, provided by a protective relaying scheme, depend to a great extent upon the type of threshold characteristics obtained from the relay unit employed in it. The selectivity, between the internal and external fault, can be achieved by the use of multizone directional distance relaying scheme with or without carrier current pilot schemes. The selectivity, between internal faults and other abnormal conditions, such as power swing etc. depend upon the shape of the threshold characteristics. The quadrilateral characteristics has proved to be the best in fulfilling these requirements to the maximum extent. The high speed clearance of faults on the complex power system network very effectively improves the transient state stability limit i.e. the power transfer capability for a given stability limit. The rotational kinetic energy introduced into a power system during a fault is proportional to the square of the fault clearance time. Therefore, high speed clearance of faults close to large sources of generation will reduce the system acceleration more than any other form of dynamic control which can be used only after the system is being accelerated. In the recent years, this aspect of improving transient stability has been drawing the

attention of quite a few research engineers and organisations. The fault clearance time depends on the speed of the protective relays as well as on that of the associated circuit breakers [1], the realization of high speed protective relaying scheme has become imperative because high speed circuit breakers are available.

Digital protection schemes are well ahead in this direction since programmable equipments are of self checking nature and fast responding type. Using programmable equipment, it is possible to realize more complex characteristics with less complexity in logic. The use of digital computer for the protection of power system equipment is of recent origin, the first proposal appearing in late 1960's. Also, very recently there has been a trend towards employing micro-processor and multiprocessor for the power system protection purposes. Microprocessors provide programmable logic at low costs. This has led protection engineers to use micro-computer in protection and other related areas which traditionally are the domains of analog devices. All these factors gave rise to the motivation for developing a microprocessor based distance relaying scheme for the protection of EHV/UHV transmission lines.

## 1.2 OBJECTIVE AND SCOPE

The objective and scope of the work reported in this thesis have been:

- a) To present a critical review of the important solid state relaying schemes reported so far for the protection of long and heavily loaded EHV/UHV transmission lines,
- b) To present an overview of the digital computer relaying algorithm developed uptill now as well as the philosophy behind the existing and proposed algorithms, and
- c) To present the design and development of the proposed microprocessor based protection schemes for the EHV/UHV transmission lines.

## 1.3 LITERATURE SURVEY

In the past, over current relays were being used for the protection of transmission lines. However, increasing demand in the use of electrical energy throughout the world has necessitated a corresponding increase in the transmission line voltage to enable to transfer move power economically and efficiently and also complexity of the power system networks, these overcurrent relays were found to be unsuitable because of several demerits such as, shifting

of balance point with the change of generation capacity, type of faults and also switching transients. Also, these over current relays can be used only on systems where the minimum fault current exceed, the maximum load current. However, the directional over current relays are still being used as back up relay for ground fault relaying. On account of the above mentioned drawbacks associated with the over current relays, the distance relays have been developed. A brief and critical review of the important literature pertaining to the evolution of distance relays, travelling wave relays, digital relays, using digital computer and microprocessor for the protection of transmission lines, is presented in the following sections.

### 1.3.1 Distance Relays:

Distance relays are used primarily for the protection of transmission lines and, as their name implies, they measure distance, i.e. they recognize faults occurring within the protected section of the line from the fact that the distance from the relay to the fault is less than the setting of the relay.

#### 1.3.1.1 Electromechanical Relay:

In the evolution of relays for the protection of transmission lines, the electromechanical relays were

developed first and in that of distance relays the plain impedance relay was first one that was conceived and developed. In 1923, Crichton [2] reported about an impedance relay which employed an induction disc actuating structure and operated in a time proportional to the impedance between the relay and the fault point. In 1928, McLaughlin and Erickson [3] reported about a directional impedance time relay built with an induction disc actuating structure. They presented the constructional details and described the principle of operation alongwith the technique for obtaining proper voltage for the restraining element. In 1944, Goldsborough [4] reported about a modified impedance relay built with a balanced beam structure and described how a circular pick up characteristic of any desired radii and with any desired location of the centre could be obtained. In 1928 the induction disc type reactance relay was designed by Warrington [5] and performance of normal and high speed reactance relay was published by George [6]. In 1933, Warrington [7] reported about a high speed reactance relay which was built with a four-pole induction cup actuating structure carrying current coils on one pair of opposite poles, and current and voltage coils on each of other poles.

Though the mho relay was first used in 1933 as the directional unit for an early type reactance relay [7], its

independent use for the protection of heavily loaded long transmission lines was first recommended in 1943 by Warrington [8] with its merits lucidly brought out. In 1944, Cordrey and Warrington [9] described its actual use in a carrier current scheme. Later, Hutchinson [10] described its use in a three step distance relaying scheme in which protection for zone 1 and 2 was provided by normal mho units and for zone 3 by an offset mho unit. In 1962, Skuderna [11] put forth the mathematical development of how offset conic and limaçon characteristics could be obtained with a four pole induction cup structure.

#### 1.3.1.2 Electronic Relay

In 1934, Wilderoe [12] presented electronic circuits, incorporating thyatron tubes, which were equivalent of many electromechanical relays in use at that time. In 1948, MacPherson and Warrington [13] described an electronic mho relay wherein instantaneous values of voltage and current inputs to the relay were compared at the instant of voltage input maximum. In 1949, Loving published electronic circuits for many protective functions, and presented experimental results. In 1954, Bergseth published a paper [14] describing an electronic directional distance relay which was insensitive to modern waveform distortion. However with the advent of solid state devices, the development of these electronic relays ceased.

### 1.3.1.3 Solid State Relays:

The first serious proposal, for employment of transistorised circuits for power system protective relaying, came from Adanson and Wedepohl [15] in 1956. In this, they presented a mathematical theory for determining the inputs necessary to obtain the directional, ohm, offset impedance and mho characteristics with a two input phase comparator. Several papers have appeared on solid state relaying using the approach of dual input comparator and multi-input cos and sine phase comparators. In 1970, Ramamoorthy and Wani [16] reported about the fabrication and test results of a solid state quadrilateral distance relay.

In 1980, Parthasarathy et.al. [17] presented a new distance relay with an adaptive pick up characteristics which has narrow tripping area during power swing conditions and which automatically expands to large area during unbalanced faults. A solid state distance relay, employing, an operational amplifier chip as an amplitude comparator and producing elliptical characteristic, was developed by Ramamoorthy et.al. [18].

### 1.3.2 Digital Relaying:

The use of digital computer, and microprocessors for protective relaying purposes has been engaging the attention of research and protection engineers since late 1960.

The first serious proposal for using digital computer came from Rockefeller [19]. The algorithms proposed so far, involves in the determination of fundamental frequency impedance to the fault point from the fundamental components of voltage and currents whichn are extracted from the complex post fault waveform by analogue and/or digital filters. Mann and Morrison [20] described the predictive calculation of peak values of and the phase angle between the voltage and current from much fewer number of samples. Several algorithms were developed subsequently and tried by Ranjabar et al. and others [26].

The possibility of utilising an on line microprocessor (micro-computer) to perform the protection, switching and data collections of EHV/UHV transmission system is attracting increased attention. Of these functions, on line protection is likely to be the most exacting in terms of micro-processor based hard wired facilities.

A directional over current relay using microprocessor was developed by A.K. Ghai [21]. The relay hardware, apart from a microcomputer, consists of simple digital circuits, current measurement is carried out with expensive analogue to digital converter. G. Thirupathaiah etc. [22] described the technique of developing a relay having quadrilateral characteristics based on fundamental frequency signal.

Y. Akimoto et.al. [23] developed a digital current differential carrier relaying using microprocessor. In 1977, Yoshiteru Miki [24] realised Mho and reactance relay characteristics and thus gave a new dimension to protection engineers in the digital relaying field.

The results, so far reported on various protection schemes for EHV/UHV transmission lines based on microprocessor application, have been obtained by simulating it on either digital computer or INTEL 8080 based microcomputer.

#### 1.4 SUMMARY OF THE WORK REPORTED IN THIS THESIS

The summary of the work carried out and reported in this thesis, is presented below chapterwise.

Chapter 2 starts with an overview of digital algorithms for protective relaying schemes of EHV/UHV transmission lines alongwith major philosophies used in designing digital relaying schemes.

Chapter 3 deals with the theory and mathematical formulation including the algorithm for the digital simulation of the proposed relaying schemes. Also, the software realization of the proposed relaying schemes are given in this chapter.

Chapter 4 deals with the design, development and testing of microprocessor based relaying schemes. Different types of digital protection systems based upon their hardware implementation have also been discussed.

Finally, the thesis concludes with Chapter 5, which highlights briefly the work reported in this thesis along with the discussion of the result and scope of further work in this field.

## CHAPTER 2

### DIGITAL PROTECTION OF TRANSMISSION LINE

#### 2.1 SUMMARY

This chapter gives an overview of digital algorithms and systems for protective relaying schemes of EHV/UHV transmission lines. Major philosophies used in designing digital relaying schemes are outlined.

#### 2.2 PRINCIPLE OF DIGITAL PROTECTION

The principle of digital protection as applied to transmission line is described by a block diagram of simplified hardware configuration as shown in Fig. 2.1. An analog input subsystem accepts 3-phase ac quantities from power system through conventional CT's and PT's. All of these quantities are sampled simultaneously at predetermined sampling rate, converted to digital form using Analog to digital converters and then transferred to the digital processor. The processor stores, organises and makes decisions based on the value of samples with reference to the programme stored in the memory of processor. The main purpose of the processor is to send the tripping command to circuit breaker for isolation of line on occurrence of internal faults.

#### 2.3 ADVANTAGES OF DIGITAL PROTECTION

The main advantages of digital protection are given below.

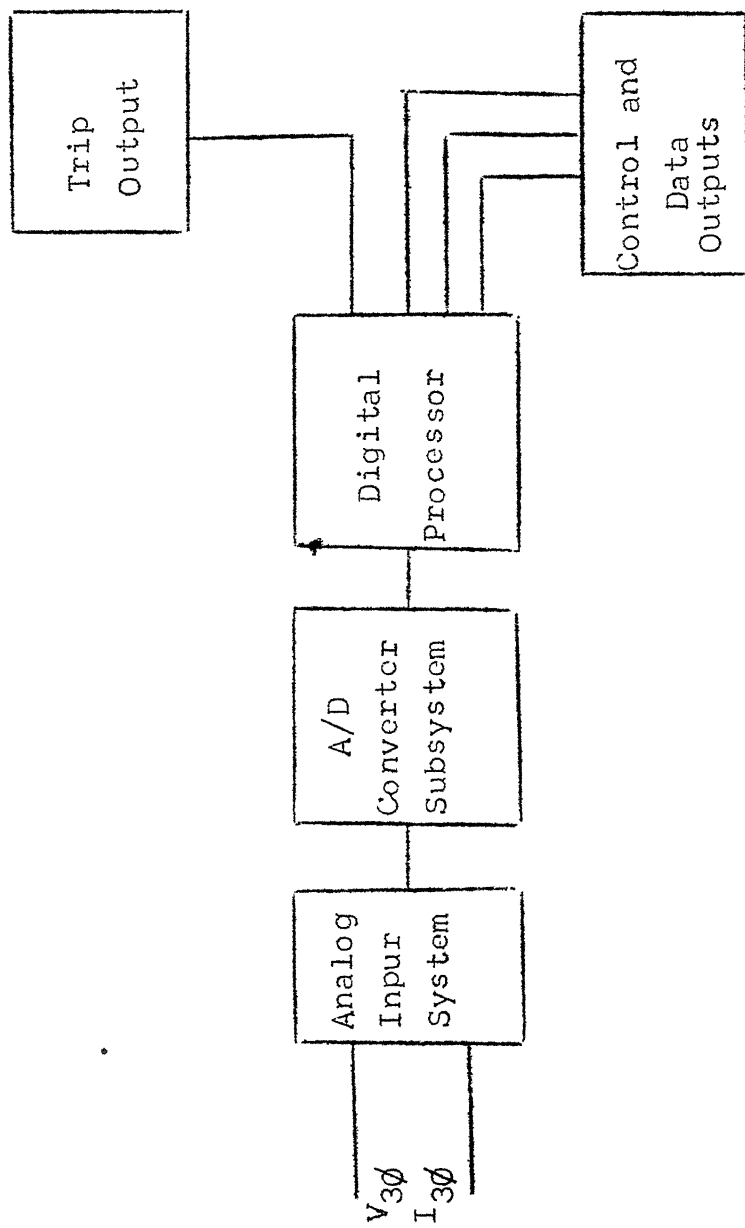


Fig. 2.1: Simplified Hardware Configuration

- a) Possibility to realize sophisticated threshold characteristics of relays.
- b) Easy to change the setting for alteration in system conditions.
- c) Ability to check correctness of input and data missing or incorrect informations.
- d) Interfacing with other controlling devices is possible.
- e) It requires less maintenance
- and f) It can give fault reports without specially designed devices, for post fault analysis.

## 2.4 DIGITAL TRANSMISSION LINE PROTECTION ALGORITHMS

Distance relays evaluate the line impedance by looking into the transmission line. The basic approaches being used in digital transmission line protection are of three types. These approaches depend on the form of the final input signal used to make the relaying decision. They are:

- a) Transmission line protection based on system parameters.
- b) Transmission line protection based on fundamental frequency signal.
- c) Transmission line protection based on the signal containing both fundamental and transient frequencies.

### 2.4.1 Transmission Line Protection Based on System Parameters:

This assumes representation of a line by a set of differential equations. The most common model of a

transmission line is the one containing R and L as system parameters. The differential equation of this model is of the form,

$$v = Ri + L \cdot \frac{di}{dt} \quad (2.1)$$

This representation of a transmission line recognises the DC offset as a valid part of the solution and, therefore, no special features have to be implemented to suppress the DC offset. Calculated value of R and L using equation (2.1) are used for phase-distance and ground-distance relaying schemes. The set of equations is manipulated depending upon the type of fault, and the final equation obtained is of the form of equation (2.1), but actually contains some combination of current and voltage phase value to form v and i given in equation (2.1).

A number of algorithms have been suggested [43] to solve equation (2.1) numerically. In 1971, McInnes et al. [25] proposed an algorithm for this purpose. It proposed integration of equation (2.1) over two successive time periods so that a sufficient number of equations are obtained to solve for R and L. Integrals are evaluated numerically using trapezoidal rule and the final expression for R and L are of the form,

$$R = \frac{(v_{k-1}+v_k)(i_{k-1}-i_{k-2})-(v_{k-1}+v_{k-2})(i_k-i_{k-1})}{(i_{k-1}+i_k)(i_{k-1}-i_{k-2})-(i_{k-1}+i_{k-2})(i_k-i_{k-1})} \quad (2.2)$$

$$L = \frac{(v_{k-1}+v_{k-2})(i_{k-1}+i_k)-(v_{k-1}+v_k)(i_{k-1}+i_{k-2})}{(i_{k-1}+i_k)(i_{k-1}-i_{k-2})-(i_{k-1}+i_{k-2})(i_k-i_{k-1})} \times \frac{h}{2} \quad (2.3)$$

where  $v$  and  $i$  are instantaneous value of voltage and current,  $k$  is the instant and  $h$  is the time interval.

However, it should be noted that, there are several problems, associated with the characteristics of actual transmission line which are not accounted in equation (2.1). This equation assumes perfectly transposed transmission line, and neither the shunt capacitance nor the capacitance used for series compensation is considered in this case. The fault resistance and effect of power flow on the line at the instant of fault are also not considered.

A number of techniques can be developed to cope with some of the problems mentioned above. Of course, a quite powerful technique is to filter the input signal with a low pass filter, which enables the attenuation of the high frequency transients which are introduced by some of the effects mentioned above.

In 1975, Ranjbar et al. [26] developed another technique which relates appropriate integration interval of equation

(2.1) to the particular harmonics that are selected for removal. The sampling rate is related as a multiple of the order of the harmonic to be removed, which makes the procedure quite restrictive by the sampling rate selection and accuracy.

If a transmission line is represented by a single PI section, then an algorithm can be developed which will accommodate both the DC offset as well as high frequency transient components of the input signals without any additional filtering. In this case, the computational burden is increased, but when this algorithm is compared to an algorithm with the low-pass filtering procedure, then the overall computational burden of the two algorithms are not very different.

#### 2.4.2 Transmission Line Protection Based on Fundamental Frequency Signal:

This relies on the theory of orthogonal transform [27]. The most widely used is the Fourier transform theory which utilizes the set of sine and cosine functions as an orthogonal set. Any function, then, can be represented as a sum of the combinations of the functions from the defined orthogonal set. Basic properties of the Fourier transform can be used to extract any particular frequency component from the incoming signal. The expression derived can be based on either

continuous or on the discrete Fourier transform. In the case of the continuous functions, some form of numerical approximation is done to obtain a digital solution. Ramamoorthy [28] correlated samples of the input signals (voltage and current) with the stored samples of reference fundamental sine and cosine waves.

If the expressions of the waveforms are given in rectangular form, then the general expressions for the sine and cosine component of voltage for sample point  $k$  are given as [29],

$$V_s = \frac{1}{N} \left[ 2 \sum_{\ell=1}^{N-1} V_{k-N-\ell} \sin \left( \frac{2\pi}{N} \ell \right) \right] \quad (2.4)$$

$$V_c = \frac{1}{N} \left[ V_{k-N} + V_k + 2 \sum_{\ell=1}^{N-1} V_{k-N+\ell} \cos \left( \frac{2\pi}{N} \ell \right) \right] \quad (2.5)$$

where  $V_i$  are the voltage samples and  $N$  is the number of samples taken per fundamental cycle and  $\ell$  is variable.

From Eqs. (2.4) and (2.5) we get the expression for voltage

$$V = \left[ V_s^2 + V_c^2 \right]^{1/2} \quad (2.6)$$

and the phase angle is given by

$$\phi_v = \tan^{-1} (V_s/V_c) \quad (2.7)$$

Similarly for current signal,

$$I = [I_s^2 + I_c^2]^{1/2} \quad (2.8)$$

and

$$\phi_I = \tan^{-1} (I_s/I_c) \quad (2.9)$$

Finally, the expression for the impedance is,

$$Z = |Z| \angle \phi_Z \quad (2.10)$$

where,

$$Z = \left[ \frac{V_s^2 + V_c^2}{I_s^2 + I_c^2} \right]^{1/2} \quad (2.11)$$

$$\phi_Z = \tan^{-1} (V/I) \quad (2.12)$$

If the calculated value of  $Z$  and  $\phi_Z$  using equations (2.11) and (2.12) exceed the setting, this determines the relaying action. This comparison can be used to perform distance impedance relaying function.

It should be noted that, theoretically, this method promises the best accuracy because it utilizes the fundamental components only and all other components are rejected. This, of course, assumes that the data are available for full power cycle. To improve the time response of the algorithm is to reduce the data window to one half of a cycle [30], which changes the limit on the expressions(2.4) and (2.5).

This introduces additional error due to DC offset and high harmonics, but the scheme can be made quite acceptable by using various methods for compensation of error sources [30]. The one half cycle scheme is particularly efficient computationally when 12 samples per cycle are used because of certain symmetries of the fourier coefficients. A sinusoidal curve fit could be performed where incoming data are used directly to calculate the apparant resistance and reactance to the fault. Samples of voltages and currents are used to perform the fundamental sinusoidal component fit [31]. Similar methods can be applied to calculate peak value of voltage and current [32] as well as power flow, which can then be used to perform relaying function.

#### 2.4.3 Transmission Line Protection Based on the Signal Containing both Fundamental and Transient Frequencies:

This scheme employs two basic techniques. One assumes that the signal can be modeled with an expression containing both fundamental signal and high frequency components. The assumed expression contains unknown parameters which can be determined by a least square estimation technique. Incoming samples are used for the fitting process. Yet another technique uses waveforms which are obtained directly from the transmission lines and contains high frequency components. These are travelling waves which can be obtained as a

solution of distributed parameter (differential) equation used as transmission line model.

The least square technique can be applied to obtain fairly good estimates, assuming a waveform which contains both decaying DC offset and harmonic components [33]:

$$K_1 e^{-\lambda t} + \sum_{m=1}^N [K_{2m} \sin(m\omega t) + K_{2m+1} \cos(m\omega t)] \quad (2.13)$$

where  $K_1, K_2, \dots, K_{2N+1}$  are unknown parameters,  $N$  is the number of harmonics to be considered,  $\lambda$  is the decay constant of the offset and  $\omega$  is the angular frequency.

Then the least square fit involves minimization of the expression

$$E = \int_0^T [I - K_1 e^{-\lambda t} - \sum_{m=1}^N [K_{2m} \sin(m\omega t) + K_{2m+1} \cos(m\omega t)]]^2 dt \quad (2.14)$$

where  $I$  is the waveform to be analyzed and  $T$  is the sampling period. The solutions of the minimization procedure are the unknown parameters  $K_r$ ,  $r = 1, 2, \dots, 2N+1$ . It should be noted that least square technique mentioned above are computationally quite involved and their accuracy is dependent on the data window applied as well as on the number of samples per cycle [29].

The travelling wave method uses as the basic model the well known telegraph equation (known as wave equation for lossless line) for distributed parameter transmission line

$$- \frac{\partial v}{\partial x} = L \frac{di}{dt} \quad (2.15)$$

$$- \frac{\partial i}{\partial x} = C \frac{dv}{dt} \quad (2.16)$$

Solution of the above equations are of the form

$$v(x,t) = \phi^+ (x-\alpha t) - Z\phi^- (x+\alpha t) \quad (2.17)$$

$$i(x,t) = \phi^+ (x-\alpha t) + \phi^- (x+\alpha t) \quad (2.18)$$

where  $L$  is the series inductance per unit length,  $C$  is the shunt capacitance per unit length,  $Z = (L/C)^{1/2}$  the line surge impedance and  $\alpha = (LC)^{-1/2}$  the velocity of propagation. The function  $\phi^+$  and  $\phi^-$  represent travelling waves which moves in the positive and negative directions respectively. However, a number of techniques are developed for operation of relay.

One approach can be based on detection of the instantaneous change in voltage and current signal at the moment of fault. A particular discriminant function can be developed which is invariant with respect to the location of fault relative to the relay terminals.

## 2.5 DISCUSSIONS ALONG WITH CONCLUDING REMARKS ON RELAYING ALGORITHMS

Comparison of the line protection algorithm has been done on a very limited scale and there is only one study that gives reasonably extensive results[29]. It was concluded [29] that, in general, any of the algorithms is perfectly accurate when the assumptions from which it is generated are considered. However, the algorithms that are based on the gross and simple assumptions about the faulted waveforms are least accurate. Also, generally, the smaller the data window is, the larger the errors are. Finally, the differential equation algorithms performed quite accurately after approximately one half of a cycle of data used. The Fourier transform algorithms are the most accurate after one cycle of the available data. The travelling wave algorithms have very quick response down to several milliseconds and are quite accurate, particularly when data are obtained from both terminals of the line.

In this thesis, the algorithms used for the proposed digital transmission line protection schemes using Microprocessor, are based on:

- a) Predictive calculation of peak value (voltage and current).
- b) Extraction of the fundamental component using Fourier transform techniques taking data window equal to one-half the power cycle.

## CHAPTER 3

### MICROPROCESSOR BASED PROPOSED RELAYING SCHEMES

#### 3.1 SUMMARY

In this chapter, the proposed methods based on two different approaches for impedance calculation for distance type protection suitable for on-line microprocessor protection of transmission lines are outlined. The software realisation of the schemes along with the computation times for implementation in real time are also given.

#### 3.2 PROPOSED RELAYING SCHEME BASED ON THE PREDICTIVE CALCULATION OF PEAK FAULT CURRENT AND VOLTAGE

The method of transmission line protection in this scheme is based on predictive calculation of peak fault current and voltage from small number of samples. The peak values of current and voltage are estimated numerically, from these the transmission line impedance is calculated and fault condition detected.

##### 3.2.1 Mathematical Formulation

The method of calculation of line impedance involves the predictive calculation of peak current and peak voltage, the impedance being determined by division of peak voltage by peak current [20]. A digital computer sampling, a sinusoidal waveform, can determine the peak as they occur.

However, it is necessary in the interest of time to determine the peak value before their occurrence i.e. to predict the peak value of the waveform from the given samples.

Let us consider a sinusoidal function,

$$v = V_{pk} \sin \omega t \quad (3.1)$$

where  $V_{pk}$  is the unknown (peak voltage) quantity and  $v$  is a typical sample value,  $\omega t$  is also unknown. Taking the derivative of (3.1) w.r.t. time we get,

$$v' = \omega V_{pk} \cos \omega t \quad (3.2)$$

where  $v'$  is determined using the numerical technique as detailed in appendix C.

From the equation (3.2) we get,

$$\frac{v'}{\omega} = V_{pk} \cos \omega t \quad (3.3)$$

Squaring eqs. (3.1) and (3.3), and adding we get,

$$V_{pk}^2 = (v)^2 + \left(\frac{v'}{\omega}\right)^2 \quad (3.4)$$

Dividing equation (3.1) by eq. (3.3) we get,

$$\begin{aligned} \frac{v\omega}{v'} &= \frac{V_{pk} \sin \omega t}{V_{pk} \cos \omega t} \\ \tan \omega t &= \frac{v\omega}{v'} \\ \omega t &= \tan^{-1} \left[ \frac{v\omega}{v'} \right] \end{aligned}$$

Thus point on cycle of voltage sample

$$V_{\theta} = \arctan \left[ \frac{V\omega}{V_r} \right] \quad (3.5)$$

Similarly for the current, we can get (refer to the eq.(3.4)),

$$I_{pk}^2 = (i)^2 + \left( \frac{i}{\omega} \right)^2 \quad (3.6)$$

$$I_{\theta} = \arctan \left[ \frac{i\omega}{I_r} \right] \quad (3.7)$$

Impedance is calculated by dividing the equation (3.4) by the equation (3.6) and hence we get,

$$Z^2 = \frac{V_{pk}^2}{I_{pk}^2} \quad (3.8)$$

Angle of impedance is obtained by subtracting equation (3.7) from the equation (3.5); hence, we get,

$$Z_{\theta} = V_{\theta} - I_{\theta} \quad (3.9)$$

The possible existence of an exponentially decaying d.c. transient on the current and voltage signal of a high voltage system is not taken into account in the impedance calculation as the offset d.c. component is negligible because if an ideal CT (having mimic impedance) connected to a secondary burden having the same X/R ratio as the primary circuit, then the voltage across the burden will be purely sinusoidal [47]. However, exact cancellation of d.c. offset is not possible for all faults. The primary X/R <sup>ratio</sup> to be matched

is that of source plus transmission line upto the fault point, and since, in general, the source  $X/R$  is not equal to the line  $X/R$ , the overall primary  $X/R$  is a variable quantity, dependent on how far along the line the fault occurs. This problem can be avoided by matching the secondary burden to the primary  $X/R$  composed of the source plus, say 90% of line impedance. It is for faults near the end of the line (i.e. near the balance point) that the most accurate impedance calculations are required for discrimination purposes and for these faults, the transient component will be almost completely removed. For faults closer in, offset will be drastically reduced but not entirely removed.

Sampling rate is a variable, but it has been taken in this case, as 40 samples per cycle, i.e. 0.5 ms between two samples, as this gives a maximum error, in  $V_{peak}$  at  $t_0$  on a 50 Hz system, of 0.15 percent (refer appendix B for details). This shows that numerical errors are at least small in theory.

### 3.2.2 General Principle of Relay for Phase Faults:

The principle used in the proposed protective scheme for phase faults is that once the disturbance in impedance is detected, the type of fault (phase or ground) is determined and a suitable single phase relaying quantities such as voltage and current are chosen for impedance calculation. Two continuous signals, one line to line voltage or line to

ground voltage and line current are sampled sequentially at predetermined sampling rate i.e. 40 samples per cycle.

Fault detection is performed by comparing the latest voltage sample to the corresponding sample of the previous cycle. If the value differs in excess of a tolerance limit 5%, the counter is incremented. If the value of the counter is equal to five, the routine jumps to fault detection zone. If the comparison of the voltage samples yield a difference less than above tolerance, the counter is decremented, if it is not already zero.

### 3.2.3 Calculation of Impedance:

On occurrence and subsequent detection of fault, the program calculates voltage and current derivatives and finally, calculate the  $V_{peak}$ ,  $I_{peak}$ , impedance and angle of impedance using the equations (3.4) - (3.9).

### 3.2.4 Software Realisation:

In the proposed relaying scheme for phase faults, a RESTRICTED MHO characteristics has been realized and simulated on intel 8080 microcomputer taking 40 samples per cycle.

For testing on Microcomputer, data has been generated using symmetrical component for the sample power network as given in the Appendix D. The algorithm used to simulate

the proposed scheme for phase faults is given below in sequence.

1. Initialize all the registers of CPU, counters etc.
2. Store the constants pertaining to relay characteristics such as set impedance, look up table for arctan.
3. Take samples.
4. Cycle by cycle comparison of voltage samples is carried out and accordingly, the counter is incremented, if, the difference in the two voltage samples is more than the specified value or otherwise decremented, if not, already zero. If the value of the counter is more than 5, fault determination starts, else go to step 3.
5. Calculate derivatives of voltage and current using numerical technique given in Appendix C.
6. Calculate  $V_{peak}$  and  $I_{peak}$  using equations (3.4) and (3.6)
7. Calculate the impedance using equation (3.8) and determine argument of impedance from the look up table of arc tan stored in the memory.
8. Check whether  $0 < Z_{\theta} < 90$  else go to step 3.
9. Check whether  $Z_R \cos(\phi - \theta) \geq Z_C$ , else go to step 3.
10. Initiate tripping signal.

The sampling is continued throughout the calculation stage and the samples are stored in the appropriate memory location by hardware arrangement discussed in the section later.

### 3.2.5 Results alongwith Discussions:

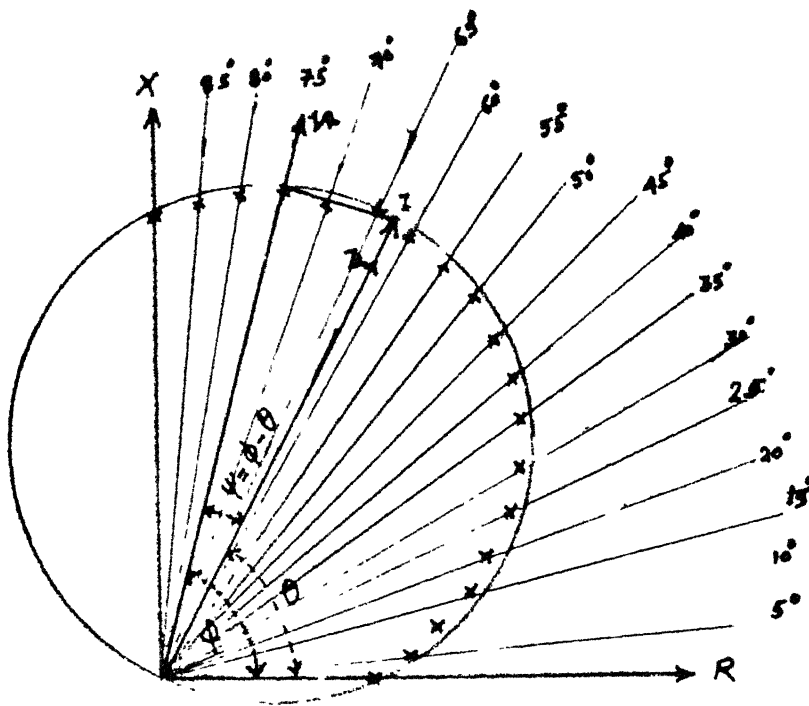
1. With the proposed algorithm the estimation of  $V_{peak}$  and  $I_{peak}$  are accurate to  $\pm 0.9\%$ , the impedance modulus to within  $\pm 10\%$  and argument of impedance to within  $5^\circ$ . Fig. 3.1 shows the characteristic of proposed algorithm, which is obtained <sup>by</sup> keeping angle  $\phi$  of  $Z_R$  fixed and for a particular angle of fault impedance, the impedance is found out where the tripping occurs and the theoretical characteristics from where it is seen that the actual characteristics is very near to the theoretical one.

2. The operating time of the proposed relaying scheme for phase faults is approximately equal to ~~4.14ms~~ for zone 1 operation, ~~15.18ms~~ for zone 2 operation and ~~25.44ms~~ for zone 3 operation, which are sum of

- a) time required to acquire 5 samples for detection of disturbance which is 2.0 ms
- b) time required for calculation of impedance and angle of impedance and computation time required to satisfy restricted Mho characteristics which is 1 8-7 cycles (2.44ms) for zone I, 13438 cycles (2.68ms) for zone II operation, 14701 cycles (2.94ms) for zone III operation

3. Timing details at various stages is given in the flow chart. (See Fig. 3.2).

4. The program listing is attached in Appendix E.



xxx CHARACTERISTIC OF PROPOSED ALGORITHM  
 — THEORITICAL CHARACTERISTIC

FIG 3.1 RESTRICTED MHO'S RELAY CHARACTERISTIC

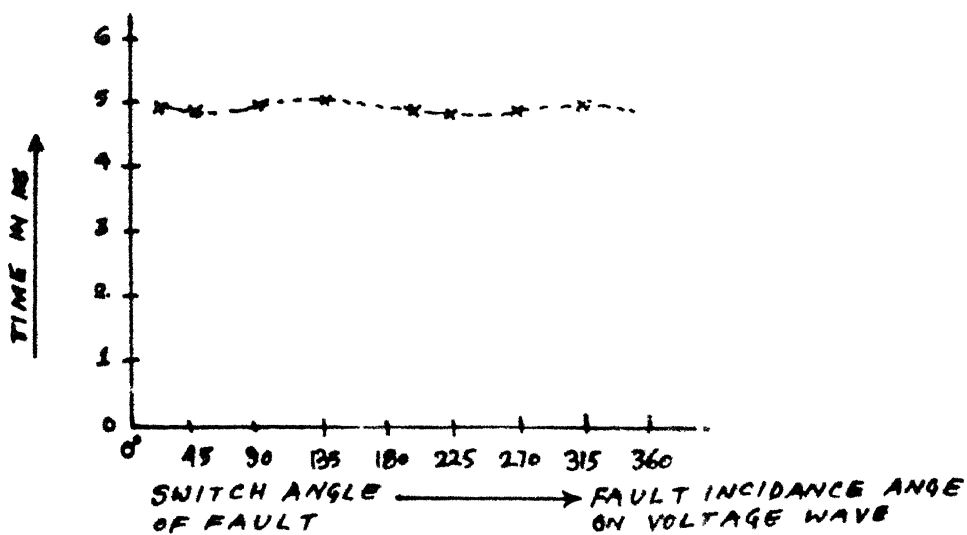


FIG 3.2A: OPERATING CHRACTERISTIC OF R.MHO RELAY

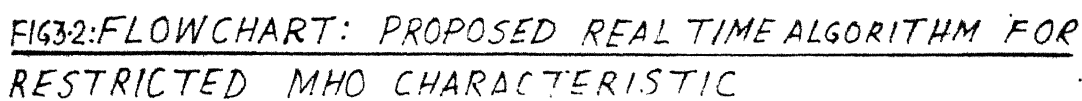


FIG 3.2: FLOWCHART: PROPOSED REAL TIME ALGORITHM FOR RESTRICTED MHO CHARACTERISTIC

5. The complexity of calculation has been reduced by converting the essentially parallel operation of analogue relays into serial digital computations. Also no data from healthy phases is involved in the calculation of impedance. This has necessitated the development of a protective scheme which, upon detection of a disturbance, isolates the phase involved and selects an appropriate set of relaying current and voltage for subsequent impedance calculation.

6. The operating time vs switch angle of fault current is given in Fig. 3.2A.

### 3.3 PROPOSED RELAYING SCHEME BASED ON FUNDAMENTAL COMPONENT TAKING DATA WINDOW EQUAL TO ONE-HALF POWER CYCLE

The proposed relaying scheme is based on the extraction of fundamental frequency component from the input signal, using Fourier transform theory and assuming that data are available for half of the power cycle.

#### 3.3.1 Mathematical Formulation:

Distance fault locating digital algorithms are often based on the processing of fundamental components which are contained in the currents and voltages. If the extraction of these components is done by means of correlating the signal with sine and cosine function of the fundamental frequency, and the data window is shorter than one cycle, the

presence of aperiodic components in the signal gives rise to large error. To minimise the error in calculating the fundamental component for a data window equal to half cycle, the signals ought to be correlated with sine/cosine functions which have periods equal to the data window length [34].

Let current and voltage input signals are represented by,

$$I(t) = I_1 \cos(\omega_1 t - \alpha) + I_a e^{-t/\tau_a} + I_p e^{-t/\tau_p} \cos(\omega_p t - \gamma) \quad (3.10)$$

$$V(t) = V_1 \cos(\omega_1 t - \alpha + \varphi) + V_a e^{-t/\tau_a} + V_p e^{-t/\tau_p} \cos(\omega_p t - \beta) \quad (3.11)$$

First terms of the right hand side of the equations (3.10) and (3.11) are steady state fundamental components. The second terms are well known aperiodic (i.e. DC) components decaying with time constant  $\tau_a$  which to a certain degree random factor like for example, a fault resistance. The third term represents decaying oscillations induced by the fault. The decaying time constant  $\tau_p$  varies and has been assumed to be equal to infinity, being the worst case. Amplitude of transient components depend on the nature of signal and, it is the transient components, which make the greatest source of error in the process of fault location. When the

data window is less than one period, the transient component becomes higher, thus increasing the overall error substantially. Therefore, the real and imaginary parts of voltage and current is calculated for the angular frequency of  $\omega_2$  corresponding to data window at which the spectrum of aperiodic component reaches minimum.

The real and imaginary parts of fundamental component of voltage and current are,

$$V_1 = V_d + jV_q \quad (3.12)$$

$$I_1 = I_d + jI_q \quad (3.13)$$

Since the signal is being processed in certain time span  $T_\omega$ , called data window, the shifted time scale is introduced into the formula of signal. This makes the middle of the window always coincide with 0 of the new time variable  $\tau$ .

Let,  $\tau = t - (t_1 + \frac{T_\omega}{2})$  where  $t_1$  is the beginning of the data window.

According to Fourier transform theory and correlating the signal with sine/cosine functions which have period equal to data window  $T_\omega$  i.e.  $\omega_2 = \frac{2\pi}{T_\omega}$ , we have,

$$V_d = \frac{K}{T_\omega} \int_{t_1}^{t_1+T_\omega} V(\tau) \cos \omega_2 \tau \, d\tau \quad (3.14)$$

$$V_q = \frac{P}{T\omega} \int_{t_1}^{t_1+T\omega} V(\tau) \sin \omega_2 \tau \, d\tau \quad (3.15)$$

$$I_d = \frac{K}{T\omega} \int_{t_1}^{t_1+T\omega} I(\tau) \cos \omega_2 \tau \, d\tau \quad (3.16)$$

$$I_q = \frac{P}{T\omega} \int_{t_1}^{t_1+T\omega} I(\tau) \sin \omega_2 \tau \, d\tau \quad (3.17)$$

where coefficients  $K$  and  $P$  [34] are

$$K = \frac{\pi(1-r^2)}{r \sin \pi r}$$

$$P = \frac{-\pi(1-r^2)}{\sin \pi r}$$

and  $r = \frac{\omega_1}{\omega_2}$

$\omega_1$  = normal power frequency of 50 hertz

$\omega_2$  = angular frequency corresponding to data window.

Taking data window equal to half the period i.e. half cycle, i.e.,  $T\omega = \pi/\omega_1$ , the coefficient  $K$  and  $P$  can be written as,

$$K = \frac{3\pi}{2}, \quad P = -\frac{3\pi}{4} \quad (3.18)$$

Equation (3.14) to equation (3.17) can be written as,

$$V_d = \frac{3\pi}{2T\omega} \int_{t_1}^{t_1+T\omega} V(t) \cos \omega_2 \left( t - t_1 - \frac{T\omega}{2} \right) dt \quad (3.19)$$

$$V_q = \frac{-3\pi}{4T\omega} \int_{t_1}^{t_1+T\omega} V(t) \sin \omega_2(t-t_1 - \frac{T\omega}{2}) dt \quad (3.20)$$

$$I_d = \frac{3\pi}{2T\omega} \int_{t_1}^{t_1+T\omega} I(t) \cos \omega_2(t-t_1 - \frac{T\omega}{2}) dt \quad (3.21)$$

and,

$$I_q = \frac{-3\pi}{4T\omega} \int_{t_1}^{t_1+T\omega} I(t) \sin \omega_2(t-t_1 - \frac{T\omega}{2}) dt \quad (3.22)$$

The solution of the above equations (3.19-3.22) have been obtained using numerical techniques as given in the Appendix A and the final results obtained are as shown below.

$$V_d = A[V(t_1) \cos \pi - 2V(t_2) \cos \frac{2\pi}{N} - 2V(t_3) \cos \frac{4\pi}{N} - \\ \dots - 2V(t_N) \cos \frac{(N-1)2\pi}{N} + V(t_{N+1}) \cos \pi]$$

$$V_q = A[V(t_1) \frac{\sin \pi}{2} + V(t_2) \sin \frac{2\pi}{N} + V(t_3) \sin \frac{4\pi}{N} + \\ \dots + V(t_N) \sin \frac{(N-1)2\pi}{N} - V(t_{N+1}) \frac{\sin \pi}{2}]$$

$$I_d = A[I(t_1) \cos \pi - 2I(t_2) \sin \frac{2\pi}{N} - 2I(t_3) \sin \frac{4\pi}{N} - \\ \dots - 2I(t_N) \cos \frac{(N-1)2\pi}{N} + I(t_{N+1}) \cos \pi]$$

$$I_q = A[I(t_1) \frac{\sin \pi}{2} + I(t_2) \sin \frac{2\pi}{N} + \sin \frac{4\pi}{N} + \\ \dots + I(t_N) \sin \frac{(N-1)2\pi}{N} - I(t_{N+1}) \sin \frac{\pi}{2}] \quad (3.23)$$

where N is the number of intervals a over a sampling period.

### 3.3.2 Fault Locating Algorithm:

The impedance seen by the relay is obtained by dividing the peak of voltage by the peak of current i.e. the expression for the impedance is,

$$\begin{aligned}
 Z &= \frac{V_d + jV_q}{I_d + jI_q} \\
 &= \frac{(V_d + jV_q)(I_d - jI_q)}{(I_d + jI_q)(I_d - jI_q)} \\
 Z &= \frac{V_d I_d + V_q I_q}{I_d^2 + I_q^2} + j \frac{V_q I_d - V_d I_q}{I_d^2 + I_q^2} \quad (3.24)
 \end{aligned}$$

But,  $Z = R + jX$

Therefore, we get,

$$\begin{aligned}
 R &= \frac{V_d I_d + V_q I_q}{I_d^2 + I_q^2} \\
 X &= \frac{V_q I_d - V_d I_q}{I_d^2 + I_q^2} \quad (3.25)
 \end{aligned}$$

### 3.3.3 Principle of Relay Operation for Phase Faults:

The principle underlying the proposed scheme is, that, the two continuous signals one, line to line voltage or line to ground voltage and second, line current are sampled sequentially at a predecided sampling rate, say 12 samples per cycle.

Fault detection is performed by comparing the latest voltage sample to the corresponding sample of the previous cycle. If the values differ in excess of a tolerance limit 5%, the counter is incremented. If the value of the counter is equal to seven (in this case) the routine jumps into the fault determination routine (see flow chart).

If the comparison of the voltage samples yield a difference less than 5% i.e. comparison is healthy, the counter is decremented, if it is not already zero.

#### 3.3.4 Calculation of Resistance and Reactance:

On detection of disturbance i.e. when counter value is equal to seven (for the present case), the program starts calculating  $R$  and  $X$  using the equation (3.25) and finding whether the fault has occurred or not. The incoming signals during this period are stored in the appropriate memory locations.

#### 3.3.5 Software Realisation:

Since quadrilateral characteristics is the best threshold characteristic available for the protection of EHV/UHV heavily loaded long lines as it encloses the fault area compactly and therefore, possesses the valuable properties of least tendency for maloperation under heavy power swings and also greatest immunity to under reaching

tendencies arising out of fault resistance. In the proposed relaying scheme for phase faults, a quadrilateral characteristics has been realized and simulated on INTEL 8080 microcomputer at IIT Kanpur taking 12 samples per cycle i.e. 6 samples per half cycle as data window is taken as half the power cycle (i.e.  $T_w = 1/2 T_1$ ).

For testing on microcomputer, data has been generated using symmetrical components (see Appendix D, for sample power system network as given in the appendix D).

The algorithm used to simulate the proposed relaying scheme for phase faults is given below with reference to the flow chart.

1. Initialize all the register of CPU, counters etc.
2. Store the constant pertaining to relay characteristics such as sine and cosine table,  $K_1$ ,  $K_2$ .
3. TAKE SAMPLES
4. Cycle by cycle comparison of voltage sample is carried out and accordingly by the counter is incremented if difference between two voltage sample is more than specified value or otherwise decremented if not already zero. If the value of counter is more than seven, fault detection starts, else Go to Step 3.
5. Calculate  $V_d$ ,  $V_q$ ,  $I_d$  and  $I_q$  using the equation (3.17-3.22) developed for data window  $T_w$  equal to half the power cycle.
6. Calculate R and X using equation (3.25).

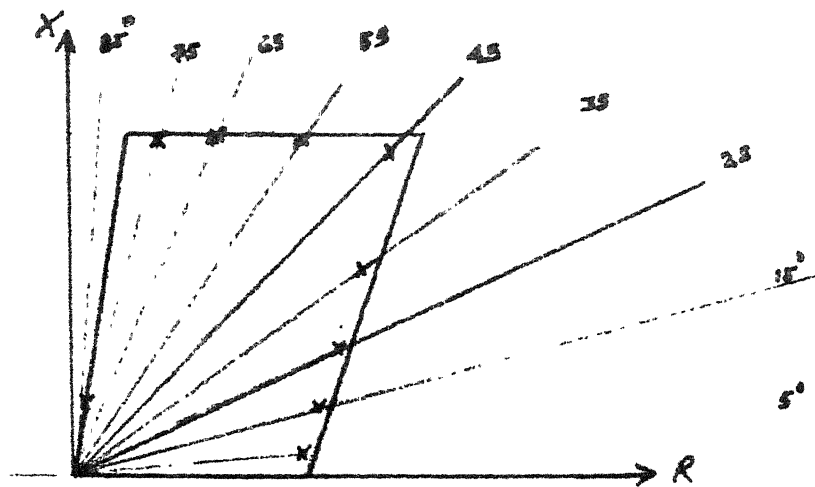
7. Check whether  $X \geq 0$  if YES continue else go to step 3.
8. Check whether  $R \geq 0$  if YES continue else go to step 3.
9. Check whether  $R \leq R_3$  if YES continue else go to, step 3.
10. Check whether  $R \leq R_2$  if YES continue else go to step 13.
11. Check whether  $R \geq R_1$  if YES continue else go to step 14.
12. Initiate the tripping signal
13. Check whether  $K_4 \geq K_2$  if YES go to Step 12 else go to step 3.
14. Check whether  $K_3 \leq K_1$  if YES go to step 12 else go to step 3.

### 3.3.6 Results and Discussions:

1. Since numerical integration is used and there is error in calculating R and X Fig. 3.3. shows the characteristics of the proposed algorithm and the theoretical characteristic, from where it can be seen, that the proposed characteristic is very close to the theoretical one.

2. The operating time of proposed relaying scheme for phase fault is approximately equal to 16.23ms for Zone 1, 21.62 ms for Zone 2 and 26.85 ms for Zone 3, which is sum of the

- a) time to acquire necessary data i.e. in this case it is 10 ms.
- b) time required for calculation of R and X and computing time required to satisfy quadrilateral characteristic which is in our case is 31026 cycle, for zone 1,  $\frac{33125}{2}$  cycle for zone 2 operation,  $\frac{34255}{2}$  cycle for zone 3 operation



x x CHARACTERISTIC OF PROPOSED ALGORITHM  
 — THEORETICAL CHARACTERISTIC

FIG 3.3: QUADILATERAL CHARACTERISTIC OF  
 THE PROPOSED RELAYING SCHEME

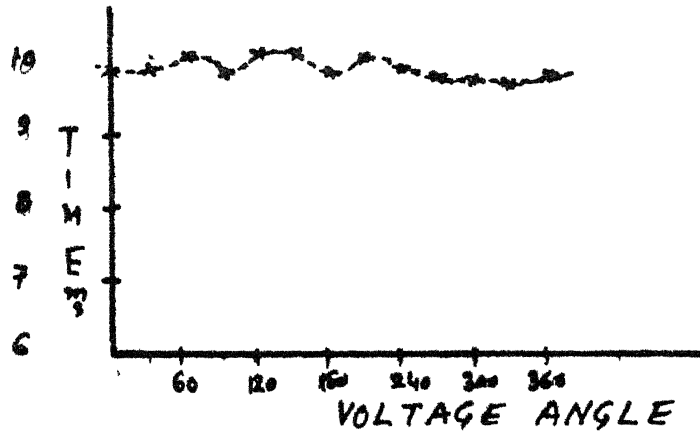
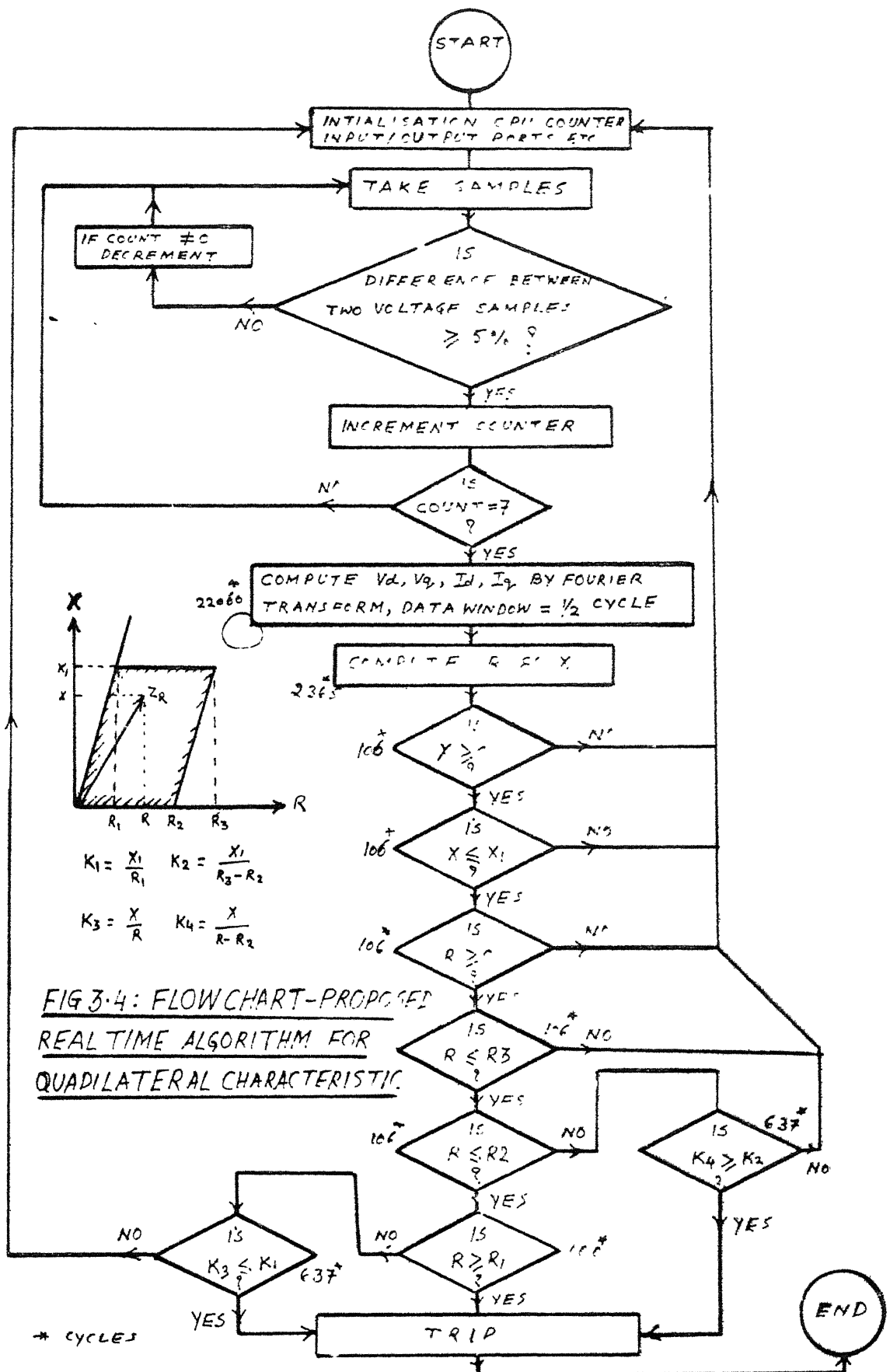


FIG 3.3A: OPERATING CHARACTERISTIC



3. Various calculation time is given in the flow chart. (See Fig. 3.4).
4. The program listing is attached as Appendix F.
5. The operating characteristic plotted between operating time and fault incidence angle is given in Fig. 3.3A.

## CHAPTER 4

### HARDWARE REALISATION OF PROPOSED RELAYING SCHEMES FOR ON LINE PROTECTION OF TRANSMISSION LINES USING MICROPROCESSOR

#### 4.1 SUMMARY

This chapter deals with the design, development and testing of microprocessor based relaying scheme. The decentralized approach has been used for the hardware realization of the proposed relaying scheme as outlined in the previous chapter.

#### 4.2 DIGITAL RELAYING SCHEMES

Based on the hardware implementation, we can divide the protection system developments into three categories.

- a) Centralized approach
- b) Decentralized approach
- c) Integrated approach

##### 4.2.1 Centralized Approach:

It covers implementation which uses only one mini-computer to accomodate most of the protection systems. The first digital relaying (prototype) system PRODAR 70, was developed in joint effort by Pacific Gas and Electric Company and the Westinghouse Electric Corporation in 1971 [35]. The system was minicomputer-based and all of the basic

protection functions found in a typical high voltage substation were implemented. For several years, a number of tests were conducted and the results were published in 1975 [36]. Also in the early 1970s, the American Electric Power Service Corporation (AEP) initiated a joint project with the IBM corporation to develop a minicomputer-based relaying and data acquisition system. This project resulted in a prototype system which was field tested and the results were published in 1976 [30]. In 1973, the General Electric Company (GEC) started a project to develop a minicomputer based distance relay, which was further extended to include a pilot scheme having a digital system at each terminal of the transmission line to be protected. Field tests for this system were completed in 1978 and the results were published in 1979 [37]. Minicomputer-based relay design activities were initiated at the University of New South Wales in early 1970s [46]. In 1976, this design was implemented by the Electricity Commission of New South Wales. The field tests started in 1978 and the results were published in 1980 [39]. Finally, a minicomputer-based protection system to be applied in low voltage substation (110 KV) was developed in Germany by the Siemens Corporation and the test results were reported in 1979 [40]. Obviously, all of the above approaches were of the centralized type since all of the functions were carried out by a minicomputer.

The final conclusions of the projects indicated, that, the idea of centralized protection system was feasible, but in order to achieve a flexible and sufficiently fast relaying function, a very fast and powerful computer system should be considered. This, in turn, implies a quite costly solution to the problem.

The above requirements for the cost-effective solution with superior performance characteristics were achieved with the introduction of microprocessor and the development of micro-computer-based relay. This led to the development of the second basic philosophy in designing digital relaying system, mainly the decentralized approach.

#### 4.2.2 Decentralized Approach:

Microprocessors have been considered for relaying application since 1975 [43]. Several projects have been initiated for the development of transmission line protection system. Prototype system for microprocessor-based distance relay were developed and field tested by the Mitsubishi Electric Corporation and the Kansai Electric Power Company [38], as well as by the Tokyo Electric Company and Toshiba Corporation [42]. A software development for a transmission line protection was reported by the Saskatchewan Power Corporation, Canada [45].

All of the above implementation were based on the concept of decentralized applications. This means that the microprocessor based system were intended to perform only one protection function. The system performed satisfactorily compared to the conventional relays. The reported system were shown to be attractive, both cost wise as well as performance wise, when compared to the conventional system. However, most of the reports related to the microcomputer - based relays were published during the period 1977-1979 and there are very few papers published on their actual field testing.

#### 4.2.3 Integrated Approach:

In this case, the protection system functions are distributed to a number of microprocessors which are then connected in an integrated manner. There are two basic types of integrated system.

- a) Integrated protection systems
- b) Integrated control and protection systems.

It should be noted that only one integrated system has been implemented [44] and tested by the Mitsubishi Electric Corporation and Kansai Electric Power Company of Japan. This is of control and protection type. This system was of a very limited scale in terms of the functions that were implemented.

The integrated systems are capable of performing the relaying functions in parallel. Each dedicated microprocessor exhibit performance characteristics which are similar to that of decentralized approach. At the same time, the system integration concept, provides the additional benefits of exclusive data acquisition and monitoring of the overall protective functions. This approach requires only a moderate system price increase when compared with the decentralized approach because of the communication subsystem. The benefits of integrated approach are numerous and include most of the benefits provided by the centralized and decentralized approaches. Some additional performance improvement is expected since the control and protection are combined and can be maintained and operated through a sophisticated man-machine interface. However, the integrated system are still in the proposal phase (state).

In the present work, the decentralized approach is used for the software/hardware system developments for the proposed relaying schemes for the protection of transmission line.

#### 4.3 BLOCK SCHEMATIC DIAGRAM OF THE PROPOSED MICROPROCESSOR-BASED RELAYING SCHEME

A simplified hardware configuration of the proposed relay is shown in the Figure 4.1 as applied for the protection of EHV/UHV transmission line.

3- $\phi$  Transmission Line

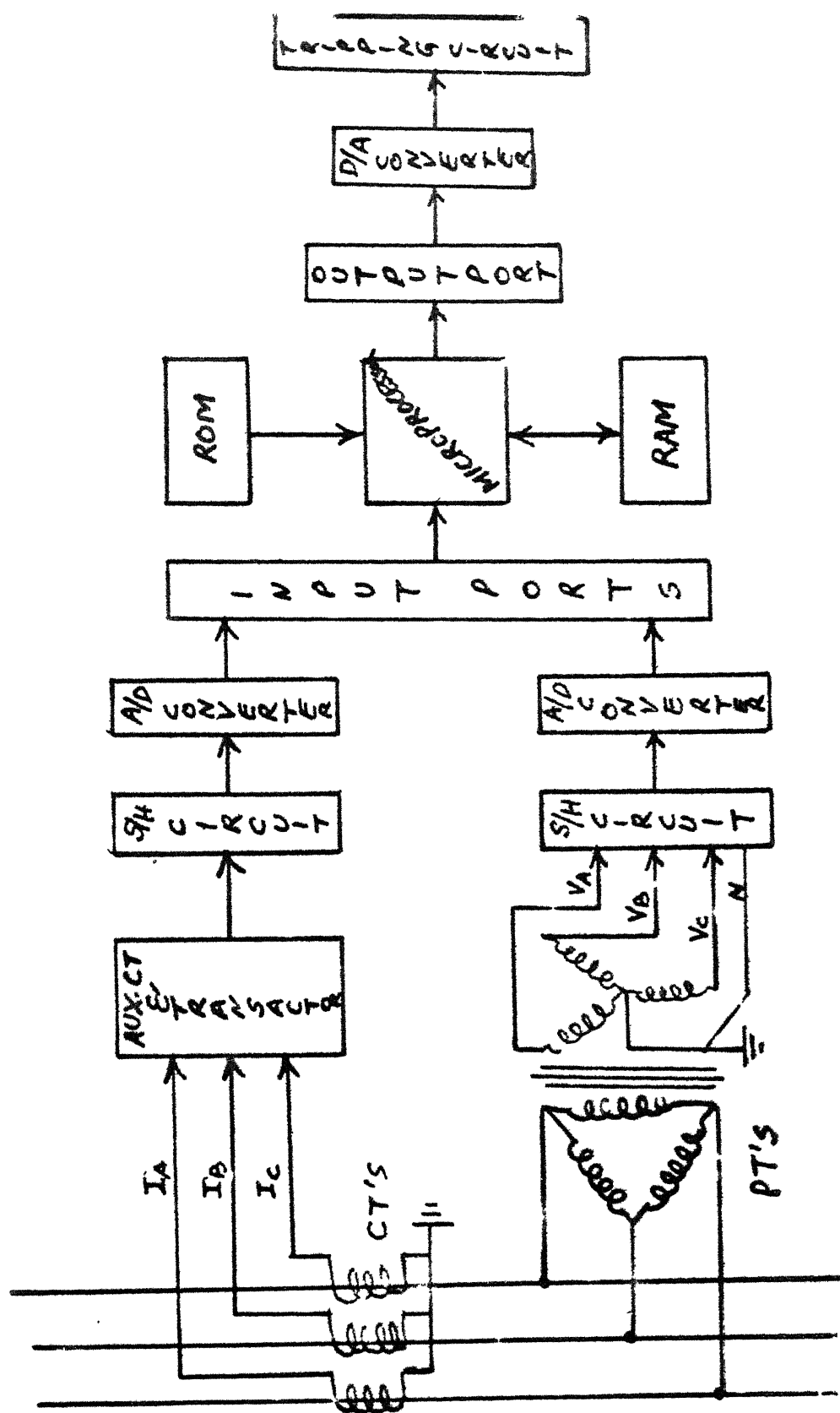


FIG 4.1: BLOCK SCHEMATIC OF THE PROPOSED RELAYING SCHEME

Data acquisition is done by sampling simultaneously the bus voltages and line currents by sample and hold circuits. These signals are converted into the digital form using Analog to digital converters and transmitted to the input ports of the microprocessor. Sampling interval is set by an external oscillator and to maintain the synchronization with the supply frequency phase locked loop (PLL) is used. The advantage of using PLL is that the sampling instant will be exactly same as that of previous cycle. The central processing unit is a microprocessor 8085 AH with a 8 bit word size. The basic cycle time is 200 nsec if crystal oscillator is of 10 MHz or 320 nsec if the crystal oscillator used is 6.144 MHz.

#### 4.4 HARDWARE REALISATION

The relay which has been developed whose schematic diagram is given in Fig. 4.1, is sub-divided into four main sections.

- a) Data acquisition system
- b) Microcomputer
- c) Secondary interface
- d) Power supply

##### 4.4.1 Data Acquisition System (DAS):

Data acquisition primarily includes circuits of





synchronization, Sample/Hold and Analogue to digital converter. The block schematic and connection diagram of data acquisition system is given in Fig. 4.2 and Fig. 4.3 respectively.

The samples are taken at an interval of 0.5 ms i.e. 40 samples/cycle. To achieve this, 2 KHz external oscillator is required. Clock of 2 KHz has been generated using PLL 4046, this clock will always be in synchronism with the supply frequency. The synchronising supply signal is fed to the input of phase lock loop (PLL) after making the output of op-amp. TTL compatible using inverter 74C901. A division by 10 counter and a division by 4 counter are provided in the feedback path of the PLL. These counters serve the purpose of providing a frequency clock ( $f_{ck} = 40 \times f$ ) at the terminals of the voltage controlled oscillator. To achieve a frequency of 600 cycle (12 samples/cycle) as required in the proposed scheme II, a counter divide by 12 is used.

The start convert pulse thus generated using PLL is given to ADC. The positive transition of start convert pulse triggers the ADC to start converting the previous sampled value into equivalent digital form. At the same time, end of conversion (EOC) status is made high putting the sampling circuit in hold mode (i.e. output of SHC is held constant in this period). After completion of the conversion, EOC is made low thereby putting the SHC in sampling mode (i.e. output

of sample and hold circuit changes during this period) and during the same time, digital data can be latched to processor through 8255. Again when the start convert pulse comes, same process is repeated.

#### 4.4.2 Microprocessor Based System:

The circuit diagram of microprocessor (8085A) based system is given in Fig. 4.4. The microprocessor based system consists of microprocessor (8085A) and its associated IC's and the memories. On board, memory consists of EPROM (2716) and RAM (2114), 8255A provides I/O ports, three 16 bit programmable timers are provided using the 8253. The address map is as follows,

RAM	:	(2114x2)	:	1 K bytes
EPROM	:	2716	:	2 K bytes
I/O Ports	:	8255A		
TIMER	:	8253		

The full size double sided PCB has been developed. Sockets have been used for all IC's to avoid trouble later while checking. After inserting the sockets, the jumpers have been wired with the hook up wires. The power supply terminals of the IC's is connected to the +5V and ground points. A 0.01  $\mu$ fd ceramic capacitor is connected between the supply terminals of the ICs. The

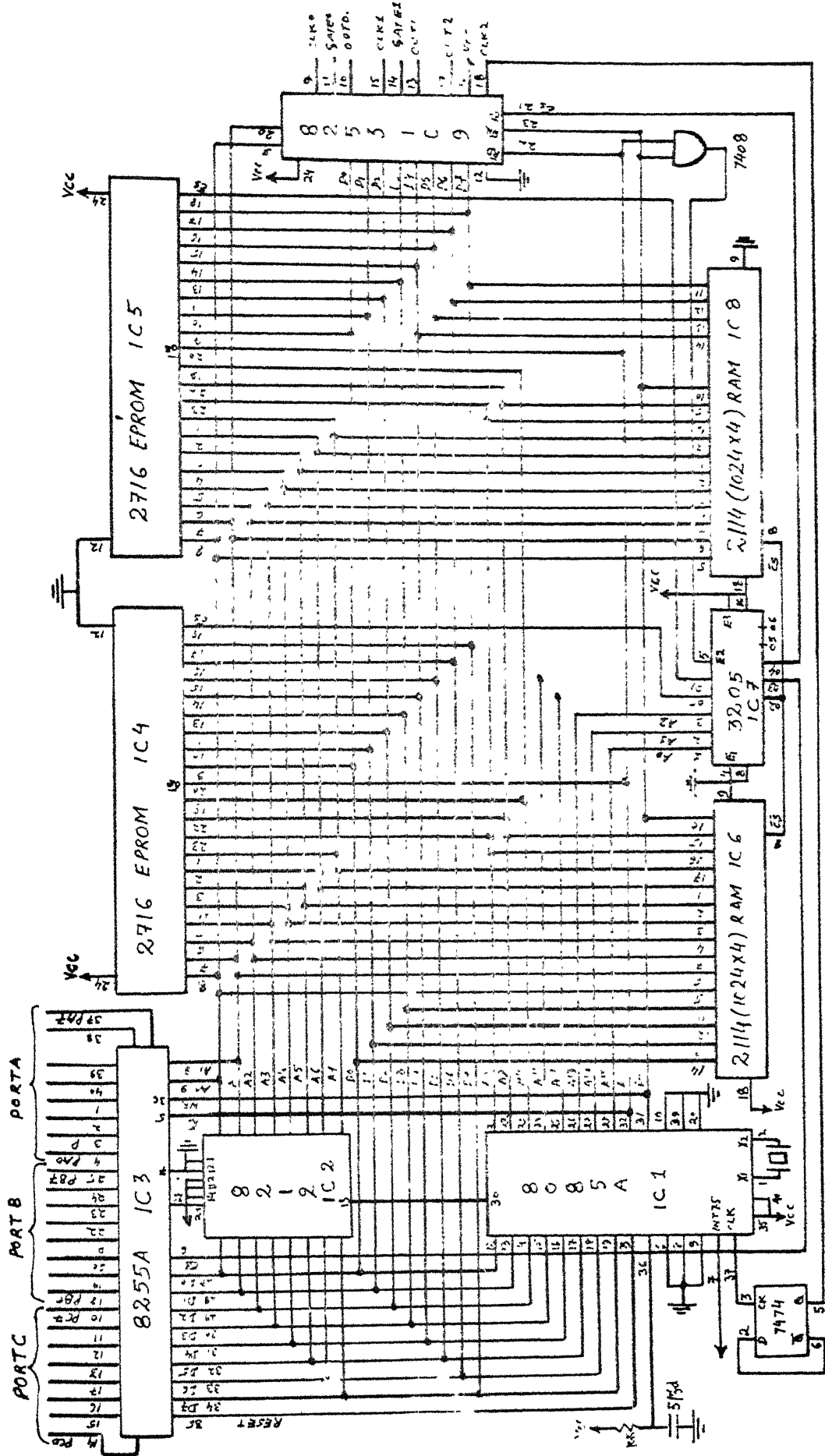


FIG 4-4 CONNECTION DIAGRAM OF MICRO-COMPUTER

6.144 MHz crystal oscillator is soldered between pin 1 and 2 of the microprocessor IC 8085A.

#### 4.4.2.1 Circuit Description:

The 8085A IC is the heart of the circuit. It needs only a single +5V supply for its working. It has built-in timing oscillator and works by connecting a crystal between terminals 1 and 2. The frequency upto which it can be worked is 10 MHz, but in the circuit 6.144 MHz crystal is used. The cycle time is approximately 320 nsecs. The 40 pins of the IC 8085A are for Address lines, Data lines, Serial input and output, interrupt pins, Hold and Hold acknowledge, Resetting input and output as well as status signal for accessing the memory ICs and input/output ports.

The lines  $AD_0$  to  $AD_7$  carry both address and data information together, on a time sharing basis. The moments during which address information is present on the line is synchronously given by the pulse coming from pin 30 - the 'Address Latch Enable' pin (shown as ALE in circuit diagram Fig. 4.4). So, by catching this information at this instant on an 8-bit latch consisting of 8-D flip-flop, the address information is continuously available on the eight output of flip-flops. The 8212 IC is used for this purpose. The input to this, are the lines  $AD_0$  to  $AD_7$ . The latched address information  $A_0$  to  $A_7$  comes out as eight lines from

8212. The  $AD_0$  to  $AD_7$  are now useful as Data lines  $D_0$  to  $D_7$  which go to the Data bus.

The address lines  $A_8$  to  $A_{15}$  are coming continuously from the pins 21, 22, 23, 24, 25, 26, 27 and 28. In this circuit, all the lines are being used i.e. all 64 K memory is being used, but at present only 2K EPROM and 1K RAM is used. The circuit works in Memory mapped mode.

The control output pins of 8085 are  $I/O \bar{M}$  (pin 34),  $\overline{RD}$  (pin 32),  $\overline{WR}$  (pin 31),  $S_0$  (pin 29) and  $S_1$  (pin 23). The control output pin  $I/O \bar{M}$ ,  $S_0$  and  $S_1$  are not used in the circuit. The  $\overline{RD}$  and  $\overline{WR}$  signals are low while some data is being read or is written to either a port or a memory location.

The address decoding is done using address decoder IC 8205. The lines  $A_{13}$ ,  $A_{14}$ ,  $A_{15}$  are given to pin  $A_0$ ,  $A_1$  and  $A_2$  of IC 8205 i.e. pin No. 1 to 3. To enable the decoder, the output after ANDING  $\overline{RD}$  and  $\overline{WR}$  using IC7400 (see Fig. 4.4) is given to enabling pin  $E_2$  (pin 5) other enabling pin 4 is grounded and pin 6 ( $E_3$ ) is connected to +5V  $V_{cc}$ . In this way, eight chip select is generated  $CS_{00}$  to  $CS_{07}$  (pin 15, 14, ..., 9 and 7). Thus, the addresses of EPROM, RAM, PPI and counter are as follows:

EPROM1 :  $CS_{00}$  : 0000H-1FFFH: 8K of memory can be address  
           : 0000H-07FFH: 2K of memory as EPROM1 is  
                           of 2K byte.

EPROM2	:	CS01	:	2000H - 3FFFH	:	Available
			:	2000H - 27FFH	:	Actual used
RAM	:	CS02	:	4000H - 5FFFH	:	Available
			:	4000H - 43FFH	:	Actual used
PPI 8255:	CS03	:	6000H - 7FFH	:	Available	
		:	6000H - 6003	:	Actual used	
TIMER	:	CS04	:	8000H - 9FFH	:	Available
			:	8000H - 8002	:	Actual used

The other pins of the 8085 which are brought out via edge connector are:

INTR, TRAP, RST 5.5, RST 6.5, RST 7.5 (interrupt pins), clock and Reset out pin.

The five interrupt pins are to be normally kept low i.e. at '0' level and when any of four is made high i.e. 1 level, any programme that is running in the microprocessor is interrupted and execute the next instruction either from a fixed location in the memory (see Table 4.1) or executes a call instruction jammed onto its buses by some external device. The call instruction is executed if INTR lines goes high. When any of these five lines goes high, we say that an interrupt has occurred. In the circuit given above in Fig. 4.4, only RST 7.5 is used and rest are grounded permanently.

Table 4.1  
Interrupt Restart Location for 8085A

LINE	Location from which next instruction is picked up ( HEX address )
TRAP	24
RST 5.5	2C ( = 5.5 x 8 )
RST 6.5	34 ( = 6.5 x 8 )
RST 7.5	3C ( = 7.5 x 8 )

The line RST 7.5 is made high periodically with reference to EOC status of A/D converter, only during the period the processor is engaged in calculation stage, to avoid the loss of any sample which are received by the ports from the data acquisition system.

The PPI (Programmable Peripheral Interface) IC 8255 is used in the circuit for Input/Output ports, which can be programmed in a variety of ways so as to suit a particular system configuration. Different operating mode of 8255 is Mode 0, Mode 1 and Mode 2. In the present system, PPI 8255 is used in Mode '0'. The 8255A PPI provides three 8 bit ports named A, B and C. The 24 lines provided, are divided into two groups: Group A and Group B. Lines in port A and four lines of port C, PC<sub>4</sub>-PC<sub>7</sub> (called the upper portion

of port C), constitute Group A and those in port B and the lower four,  $PC_0 - PC_3$ , in port C constitute Group B. Each port can be programmed to be either an input or an output port. Also, port A can be used as a bidirectional bus for input/output.

#### 4.4.3 Power Supply System:

A +5V power supply is required for the microprocessor system and a total current of about 500 mA will be needed. Data acquisition system requires a +5V, -5V, +15V and -15V power supply and current requirement is approximately 400 mA.

#### 4.5 LABORATORY TESTING

The software programmes developed in Chapter 3 for the proposed relaying schemes for transmission line protection are stored separately in different EPROM and each scheme is tested and relay has correctly tripped the line, the tripping of line is indicated by glowing of LED.

In steady state, the interrupt 7.5 is always kept low as processor is primarily engaged for receiving samples and comparison thus of, as for the programmes. On occurrence of disturbance on the system, the processor enters into a fault routine, to avoid to lose any sample during the period of computation, the interrupt 7.5 is enabled and processor

is interrupted by the EOC status of A/D converter at a frequency approximately equal to the sampling frequency.

The dynamic testing of the relay to investigate the transient over-reach and accuracy/range curves, could not be performed because of limited facilities available.

The operating specification of the relay is as

Voltage signal (from PT's) : +5V to -5V AC maximum

Current signal (from CT's) : +5V to -5V AC maximum

Supply requirements : +5V DC  
+15V DC  
-15V DC  
- 5V DC

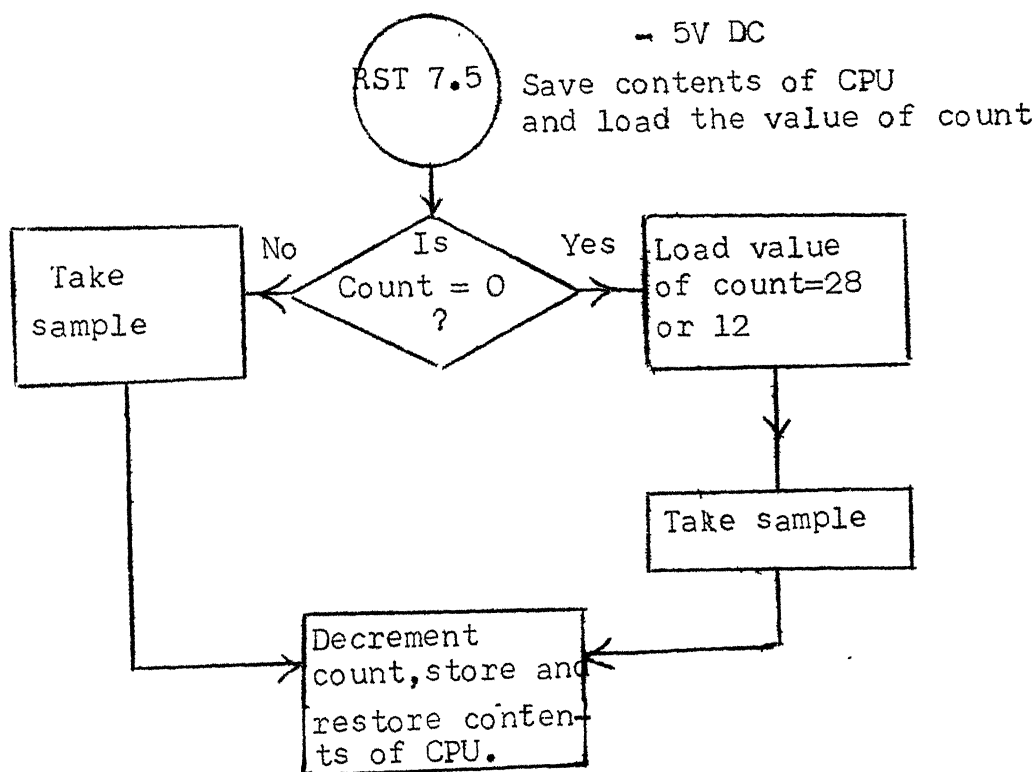


Fig. 4.5: Flow Chart 7.5 Interrupt Service Routine

## CHAPTER 5

### CONCLUSION

#### 5.1 GENERAL

EHV and UHV transmission system needs a reliable, fast, efficient and low cost protection schemes, in order to transmit power reliably. Protection schemes using digital computers is a step ahead in this direction, as it is capable of realising complex threshold characteristics with lesser complexity and is of self checking nature. Accordingly, the primary objective of this thesis has been the design and development of microprocessor based protective relaying scheme. In the following sections, a brief account of the work carried out in this thesis, and also the scope for further work, are presented.

#### 5.2 REVIEW OF THE WORK CARRIED OUT IN THIS THESIS

The protection schemes proposed in this thesis, are based upon the following two approaches:

- a) Predictive calculation of peak fault current and voltage from a small number of sample values.
- b) Fundamental component method taking samples for one-half power cycle.

In the proposed relaying scheme I, the software for realising three zone restricted Mho's relay characteristics has been developed which has been tested on a sample power system (see appendix D ). The total operating time of relay from the instant the fault occurs is 4.94 ms for zone I, 15.18ms for zone II and 25.44 ms for zone III. That is, the fault in zone I is cleared in less than a quarter cycle (5 ms).

In the proposed relaying scheme II, the software for realising three zone quadrilateral characteristics has been developed and tested on a sample power system network (see Appendix D). The total operating time from the instant the fault occurs is 16.23 ms for zone I, 21.62 ms for zone II and 26.85 ms for zone III. That is, a fault in zone I is cleared in approximately one power cycle.

For the hardware realization of the above schemes, the relay based on microprocessor 8085 has been fabricated and tested. The relays comprises mainly, synchronising circuit; data acquisition system having sample/hold and analogue to digital converters; micro-computer using 8085A microprocessor. Provision exists for adding more memory and input/output ports if the situation demands. Visual display of the calculated fault impedance, distance to the fault point and type of fault can be obtained by interfacing TTY to the relay.

Any type of threshold characteristics such as that of plane impedance, direction relay, conical, hyperbola and over current relay can be obtained by developing the appropriate software.

### 5.3 SCOPE FOR FUTURE WORK

The proposed schemes, in single phase application, can be used for line to ground fault and in a three phase system, it can be used either for line to ground fault or phase to phase faults. However, the proposed relaying scheme can be extended for the discrimination of all the types of faults in three phase or multiphase system by using multiplexer and Direct Memory Access (DMA).

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## APPENDIX A

### NUMERICAL INTEGRATION

The general problem of numerical integration may be stated as follows. Given a set of data points  $(x_0, y_0)$ ,  $(x_1, y_1), \dots, (x_n, y_n)$  of a function  $y = f(x)$  where  $f(x)$  is not known explicitly, it is required to compute the values of definite integral,

$$I = \int_a^b y \, dx \quad (A.1)$$

Let the interval  $[a, b]$  be sub-divided into  $N$  equal subinterval, such that,  $a = x_0 < x_1 < x_2 < \dots < x_N = b$  clearly  $x_n = x_0 + Nh$  where  $h$  is the step size (i.e. length of interval). Hence the integration becomes

$$I = \int_{x_0}^{x_N} y \, dx \quad (A.2)$$

Consider the figure A.1. Let the samples are taken at a uniform interval. If the interval is small, then the area enclosed by two samples is approximately of

quadilateral form. Then the total area enclosed by the curve over a definite period  $x_0, x_1$  is given by,

$$I_1 = \int_{x_0}^{x_1} y dx = h [y_0 + y_1] \quad (A.3)$$

Generalising it for the interval  $[a, b]$ , we get,

$$\begin{aligned} I &= \int_{x_0}^{x_1} y dx + \int_{x_1}^{x_2} y dx + \dots + \int_{x_{N-1}}^{x_N} y dx \\ &= \frac{h}{2} [y_0 + 2(y_1 + y_2 + \dots + y_{N-1}) + y_N] \end{aligned} \quad (A.4)$$

which is known as Trapezoidal rule.

To evaluate  $V_d$ ,  $V_q$ ,  $I_d$  and  $I_q$  numerically, the above trapezoidal rule is applied. From equation (3.19) thus we get,

$$V_d = \frac{3\pi}{2Tw} \int_{t_1}^{t_1+Tw} V(t) \cos \omega_2(t - t_1 - \frac{Tw}{2}) dt \quad (A.5)$$

Here  $Tw$  = time period =  $b-a = Nh$

$$\begin{aligned} V_d &= \frac{3\pi}{2xNh} \times \frac{h}{2} [V(t_1) \cos \omega_2(t_1 - t_1 - \frac{Tw}{2}) + 2V(t_2) \cos \omega_2 \\ &\quad (t_2 - t_1 - \frac{Tw}{2}) + 2V(t_3) \cos \omega_2(t_3 - t_1 - \frac{Tw}{2}) + \dots \\ &\quad + 2V(t_N) \cos \omega_2(t_N - t_1 - \frac{Tw}{2}) + V(t_{N+1}) \cos \omega_2(t_{N+1} - t_1 - \frac{Tw}{2})] \end{aligned}$$

Since  $Tw = 2\pi/\omega_2$ .

$$V_d = \frac{+3\pi}{4N} [V(t_1)\cos(-\pi) + 2V(t_2)\cos(\frac{2\pi}{N} - \pi) + 2V(t_3)\cos(\frac{4\pi}{N} - \pi) + \dots \\ + 2V(t_N)\cos(\frac{(N-1)\pi}{N} - \pi) + V(t_{N+1})\cos(+\pi)] \quad (A.6)$$

Similarly, for

$$V_q = \frac{-3\pi}{8N} [V(t_1)\sin(-\pi) + 2V(t_2)\sin(\frac{2\pi}{N} - \pi) + 2V(t_3)\sin(\frac{4\pi}{N} - \pi) + \dots \\ + 2V(t_N)\sin(\frac{(N-1)2\pi}{N} - \pi) + V(t_{N+1})\sin(\pi)] \quad (A.7)$$

$$I_d = \frac{+3\pi}{4N} [I(t_1)\cos(-\pi) + 2I(t_2)\cos(\frac{2\pi}{N} - \pi) + 2I(t_3)\cos(\frac{4\pi}{N} - \pi) + \dots \\ + 2I(t_N)\cos(\frac{(N-1)2\pi}{N} - \pi) + I(t_{N+1})\cos(\pi)] \quad (A.8)$$

$$I_q = \frac{-3\pi}{8N} [I(t_1)\sin(-\pi) + 2I(t_2)\sin(\frac{2\pi}{N} - \pi) + 2I(t_3)\sin(\frac{4\pi}{N} - \pi) + \dots \\ + 2I(t_N)\sin(\frac{(N-1)2\pi}{N} - \pi) + I(t_{N+1})\sin(\pi)] \quad (A.9)$$

Introducing  $\frac{3\pi}{4N} = A$  constant and after simplification, we get,

$$V_d = A[V(t_1)\cos\pi - 2V(t_2)\cos\frac{2\pi}{N} - 2V(t_3)\cos\frac{4\pi}{N} - \dots \\ - 2V(t_N)\cos\frac{(N-1)2\pi}{N} + V(t_{N+1})\cos\pi] \quad (A.10)$$

$$V_q = A[V(t_1)\frac{\sin\pi}{2} + V(t_2)\sin\frac{2\pi}{N} + V(t_3)\sin\frac{4\pi}{N} + \dots \\ + V(t_N)\sin\frac{(N-1)2\pi}{N} - V(t_{N+1})\frac{\sin\pi}{2}] \quad (A.11)$$

$$\begin{aligned}
 I_d = A[ & I_{(t_1)} \cos \pi - 2I_{(t_2)} \cos \frac{2\pi}{N} - 2I_{(t_3)} \cos \frac{4\pi}{N} - \dots \\
 & - 2I_{t_N} \cos \frac{(N-1)2\pi}{N} + I_{(t_{N+1})} \cos \pi] \quad (A.12)
 \end{aligned}$$

$$\begin{aligned}
 I_q = A[ & I_{t_1} \frac{\sin \pi}{2} + I_{(t_2)} \sin \frac{2\pi}{N} + I_{(t_3)} \sin \frac{4\pi}{N} + \dots \\
 & + I_{(t_N)} \sin \frac{(N-1)2\pi}{N} - I_{(t_{N+1})} \frac{\sin \pi}{2} ] \quad (A.13)
 \end{aligned}$$

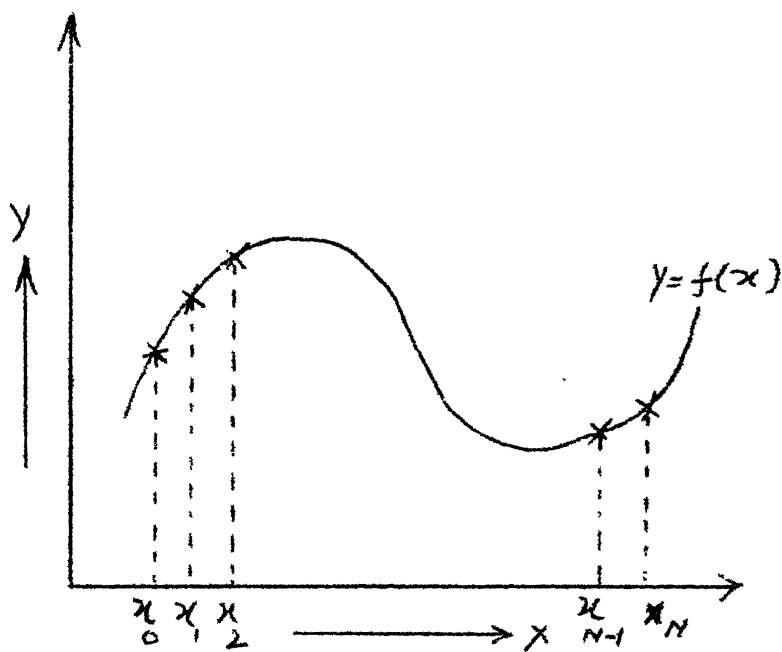


Fig. A-1

## APPENDIX B

### SELECTION OF SAMPLING RATE

Assume that the waveforms are sampled at an interval of  $\Delta t$  with actual sampling times being  $t_k, t_{k+1}, \dots$  and corresponding sampled value being  $v_k, v_{k+1}, \dots$ . Take  $t_0$  as being half way between  $t_k$  and  $t_{k+1}$ . Then we get,

$$v_0 = \frac{1}{2} (v_k + v_{k+1}) \quad (B.1)$$

$$v'_0 \approx \frac{\Delta v}{\Delta t} = \frac{1}{\Delta t} (v_{k+1} - v_k) \quad (B.2)$$

Since from (3.4) we know that,

$$v_{pk}^2 = (v)^2 + \left(\frac{v'}{\omega}\right)^2 \quad (B.3)$$

So, this yields an estimate  $V_0$  of  $V$  at time  $t_0$  as

$$V_0^2 = v_0^2 + \left(\frac{\Delta v}{\omega \Delta t} \Big|_{t=t_0}\right)^2 \quad (B.4)$$

Put the value of  $v_0$  and  $\Delta v / \Delta t$  from equations (B.1) and (B.2) into equation (B.4) we get,

$$\begin{aligned} V_0^2 &= \left[ \frac{1}{2} (v_k + v_{k+1}) \Big|_{t=t_0} \right]^2 + \left[ \frac{v_{k+1} - v_k}{\omega \Delta t} \Big|_{t=t_0} \right]^2 \\ &= \frac{v_{pk}^2}{4} \left[ \sin \omega t_0 - \frac{1}{2} \omega \Delta t + \sin(\omega t_0 + \frac{1}{2} \omega \Delta t) \right]^2 + \frac{v_{pk}^2}{(\omega \Delta t)^2} \times \\ &\quad \left[ \sin(\omega t_0 + \frac{1}{2} \omega \Delta t) - \sin(\omega t_0 - \frac{1}{2} \omega \Delta t) \right]^2 \end{aligned}$$

Expanding the above and neglecting the high order term for sake of simplicity we get,

$$V_o = V_{pk} \left[ 1 - \frac{\omega^2 (\Delta t)^2}{4} \sin^2 \omega t_o + \dots \right] \quad (B.5)$$

For  $\Delta t = 0.5$  ms, the equation (B.5), gives a maximum error in  $V_o$  on 50 Hz system of 0.15%, numerical analysis list the several ways of calculating the derivative [48]-[50]. In general, these methods are series expression of forward, backward or central differences. The actual formula for numerical differentiation can be obtained by differentiating the interpolating polynomial, i.e. interpolation formula. Isaacs and Keeler [90] have shown that interpolation error are least near the centre of interval of interpolation which is equivalent of using interpolating formula developed using central difference. But it is advantageous, for real time implementation, to use backward difference for calculating the derivative using existing samples. These consideration led to the tentative selection of a sampling interval of 0.5 ms i.e. 40 samples per cycle.

## APPENDIX C

### DIFFERENTIATION FORMULAS

Using the standard notation  $\nabla$ ,  $\delta$  and  $\mu$  for the operation of backward differencing, central differencing and averaging respectively, the basic central difference expression for derivative [49] is

$$hy'_k = (\mu \delta - \frac{1}{6} \mu \delta^3 + \frac{1}{30} \mu \delta^5 - \dots) y_k \quad (C.1)$$

where  $h = \Delta t$  and  $y$  stands for  $v$  and  $i$  respectively.

Using the first term only of the above result (eqn.C.1) we get,

$$hy'_k = \frac{1}{2} (y_{k+1} - y_{k-1}) \quad (C.2)$$

And using also the second term of above result (eqn. C-1) we get,

$$hy'_k = -\frac{1}{12} (y_{k+2} - \frac{2}{3} y_{k+1} - \frac{2}{3} y_{k-1} + \frac{1}{12} y_{k-2}) \quad (C.3)$$

the backward differences expression for derivative [49] is,

$$hy'_k = (\nabla - \frac{1}{2} \nabla^2 - \dots) y_k \quad (C.4)$$

Using the first term only of result (eqn. C.4) we get,

$$hy'_k = y_k - y_{k-1} \quad (C.5)$$

And using also the second term of the result (eqn. C.4) we get,

$$hy'_k = \frac{1}{2} (y_k - y_{k-2}) \quad (C.6)$$

From the above, it is clear, that, the expression at (C.2), (C.3) require sample value at times later than  $t_k$ , whereas expression (C.5) and (C.6) do not. Thus any of central difference and backward difference can be considered as possible ways of calculating the derivative.

## APPENDIX D

### TRANSMISSION LINE DATA [26]

Base	= 230 KV, 1000 MVA
Length of line	= 300 miles
Line Parameters:	
Positive sequence reactance	= $j0.123 \times 10^{-2}$ p.u.
Positive sequence resistance	= $0.223 \times 10^{-3}$ p.u.
Zero sequence resistance	= $1.226 \times 10^{-3}$ p.u.
Zero sequence reactance	= $j0.32 \times 10^{-3}$ p.u.
Positive sequence capacitive reactance	= -j420 p.u.
Zero sequence capacitive reactance	= -j714 p.u.
Source impedance $Z_s$	= $0.033 + j0.315$

```

=====
; REAL TIME MICROPROCESSOR BASED PROGRAMME FOR
; THREE ZONE RESTRICTED MAIN RELAY
=====
; ASSIGNMENT MEMORY LOCATION FOR VARIABLES
;
; DATUM EQU 4000H ; SAMPLES OF VOLTAGE & CURRENT
; COSTA EQU 0490H ; COS LOOK UP TABLE
; PORTV EQU 8000H ; PORT 1 FOR VOLTAGE SAMPLES
; PORTI EQU 8001H ; PORT 2 FOR CURRENT SAMPLES
; RANGE EQU 0410H ; RANG LOOK UP TABLE
; AMPLA EQU 4056H
; VAMPL EQU 4057H ; STORING THE ANGLE OF VOLTAGE
; IAMPL EQU 4058H ; STORING THE ANGLE OF CURRENT
; FIRST EQU 4059H ; STORING VALUE OF VPEAK SQUARE
; SECOND EQU 405CH ; STORING VALUE OF IPEAK SQUARE
; THIRPO EQU 405EH ; USED AS TEMPORARY STORAGE
; FORTH EQU 4060H
; FIFTH EQU 4062H
; INTIC EQU 4064H
; BASE EQU 4065H ; USED AS TEMPORARY STORAGE
; VBASE EQU 4066H
; PORTC EQU 8002H ; CONTROL PORT OF PPI
; CNPPI EQU 8003H ; CONTROL WORD OF PPI
; VOERI EQU 4067H ; STORING VOLTAGE DERIVATIVE
; ; CURRENT, CURRENT DERIVATIVE
=====
ORG 0000H
LXI SP, 42FFH
; *****
; INITIALISATION OF INPUT/OUTPUT PORTS COUNTERS
; *****
MVI A, 93H ; PORTA=INPUT, PORTB
; PORTC LOWER=INPUT
; PORTC UPPER=OUTPUT
STA CNPPI
MVI A, 02H
STA AMPLA
MVI A, 00H
STA PORTC
LXI H, DATUM
MVI C, 28H
FLAKE: LDA PORTC
RAR
JC LAMB
JMP FLAKE
LAMB: LDA PORTV
CALL DELHI
MOV M, A
INX H
LDA PORTI
CALL DELHI
MOV M, A
DCR C
JZ FRESH
JMP FLAKE
NOP
NOP
NOP
NOP
NOP
NOP
RST75 : PUSH PSW
PUSH H
PUSH D
LDA INTIC
CPI 0H
JZ HOLDG
MOV D, A
MVI A, 28H
SUB D
LXI H, DATUM
MOV E, A
MVI D, 0H
DAO D
LDA PORTV
CALL DELHI

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01800

0058	77	MOV M,A
0059	36800	JMP VERRKT
005C	3E28	HOLDG: MVI A,28H
005E	325440	SIA INTIC
0061	210040	LXI H,DATUM
0064	340060	LDA PORTV
0067	CD6503	CALL DELHI
006A	77	MOV M,A
006B	01	VERKT: POP D
006C	21	POP H
006D	21	POP PSW
006E	03	RET
006F	3A6440	ORIGIN: LDA INTIC
0072	4F	MOV C,A
0073	3E28	MVI A,28H
0075	91	SUB C
0076	210040	LXI H,DATUM
0079	5F	MOV E,A
007A	1600	MVI D,0H
007C	19	DAD D
007D	1600	MVI E,0H
007F	C3A100	JMP SAMPL

-----  
COLLECTION OF SAMPLES OF VOLTAGE AND CURRENT AND  
CYCLE BY CYCLE COMPARISON OF VOLTAGE SAMPLES AND  
REPLACING THE PREVIOUS BY LATEST SAMPLES OF VS C  
-----

0082	1500	FRESH: MVI E,00H
0084	3E28	MVI C,28H
0086	210040	LXI H,DATUM
0089	C3A100	JMP SAMPL
008C	23	INCR: INX H
008D	00	DCR C
008E	CA8200	JZ FRESH
0091	C3A100	JMP SAMPL
0094	3E00	DECRE: MVI A,0H
0096	9B	CMP E
0097	CA9800	JZ GHOST
009A	10	DCR E
009B	AF	GHOST: XRA A
009C	23	INX H
009D	00	DCR C
009E	CA8200	JZ FRESH
00A1	46	SAMPL: MOV B,M
00A2	3A0260	BOTHM: LDA PORTC
00A5	1F	RAR
00A6	DAAC00	JC DOWNR
00A7	C3A200	JMP BOTHM
00AC	3A0060	DOWNR: LDA PORTV
00AF	CD6503	CALL DELHI
00B2	77	MOV M,A
00B3	23	INX H
00B4	3A0160	LDA PORTT
00B7	CD6503	CALL DELHI
00BA	77	MOV M,A
00BB	2B	DCX H
00BC	7B	MOV A,B
00BD	55	MOV D,M
00BE	8A	CMP D
00BF	DAC500	JC LOCK
00C2	C3C900	JMP KEY
00C5	47	LOCK: MOV B,A
00C6	7A	MOV A,D
00C7	50	MOV D,B
00C8	92	KEY: SUB D
00C9	1605	MVI D,05H
00CB	8A	CMP D
00CC	DAD200	JC MAXX
00CF	C3D700	JMP SOLO
00D2	AF	MAXX: XRA A
00D3	23	INX H
00D4	C39400	JMP DECRE
00D7	10	SOLO: INR E
00D8	3E02	MVI A,02H



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 0148 325540  
 0148 70  
 0148 44  
 0150 215940  
 0153 77  
 0154 23  
 0155 78  
 0156 77  
 0157 71  
 0159 23  
 0159 230E01  
 0157 32  
 0157 32  
 015E 325540  
 0161 70  
 0162 44  
 0163 215C40  
 0166 77  
 0167 23  
 0168 78  
 0169 77  
 016A E1  
 016B 28  
 016C 28  
 016D 23

INP PONES  
 STOPS: STA AMDA  
 MOV A, L  
 MOV R, H  
 LXT H, FIRST  
 MOV M, A  
 INX H  
 MOV A, R  
 MOV M, A  
 POP H  
 INX H  
 INP TIME  
 STOPS: INR A  
 INR A  
 STA AMDA  
 MOV A, L  
 MOV R, H  
 LXT H, SECND  
 MOV M, A  
 INX H  
 MOV A, R  
 MOV M, A  
 POP H  
 DCX H  
 DCX H

-----  
 ; CALCULATE RATIO OF R = ( / ) = 32 / OBTAINED AS  
 ; 0.32 / \*100 = 32 / ( ) TO GET ANGLE  
 ; CALCULATE RATIO OF VOLTAGE / VOLTAGE DERIVATIVE/  
 ; AND FOR CURRENT DIVIDED BY CURRENT DERIVATIVE/  
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016E 73  
 016F 0820  
 0171 33  
 0172 307703  
 0175 40  
 0176 44  
 0177 31  
 0178 23  
 0179 38  
 017A 1600  
 017C E5  
 017D 308703  
 0180 39  
 0181 30  
 0182 E1  
 0183 0E00  
 0185 7A  
 0186 E607  
 0188 1F  
 0189 0A9701  
 018C 1F  
 018D 0AA101  
 0190 1F  
 0191 0AAB01  
 0194 03AF01  
 0197 0C  
 0198 3F  
 0199 1F  
 019A 0AA101  
 019D 3F  
 019E 039D01  
 01A1 0C  
 01A2 0C  
 01A3 3F  
 01A4 1F  
 01A5 0AAB01  
 01A8 03AF01  
 01AB 0C  
 01AC 0C  
 01AD 0C  
 01AE 0C  
 01AF 3800

NATH : MOV A, M  
 MVI B, 20H  
 PUSH H  
 CALL MULTI  
 MOV C, L  
 MOV R, H  
 POP H  
 INX H  
 MOV E, M  
 MVI D, 00H  
 PUSH H  
 CALL VISON ; REG. B-C CONTAINS QUOTIENT  
 MOV E, C  
 MOV D, B  
 POP H  
 MVI C, 00H  
 MOV A, D  
 ANI 00000111B  
 RAR  
 JC NAMAK  
 RAR  
 JC HARAM  
 KISAN : RAR  
 JC ARMAN  
 JMP KUTAB  
 NAMAK : INR C  
 CMC  
 RAR  
 JC HARAM  
 CMC  
 JMP KISAN  
 HARAM : INR C  
 INR C  
 CMC  
 RAR  
 JC ARMAN  
 JMP KUTAB  
 ARMAN : INR C  
 INR C  
 INR C  
 KUTAB : MVI A, 00H

03570	01B1	39	CMP C
03580	01B2	3AD001	JZ KARZ
03590	01B5	3301	MVI A, 01H
03600	01B7	39	CMP C
03610	01B8	3AR501	JZ KARAM
03620	01B8	3302	MVI A, 02H
03630	01B9	39	CMP C
03640	01BE	3AF201	JZ GANDI
03650	01C1	3373	MVI A, 03H
03660	01C3	39	CMP C
03670	01C4	3A0002	JZ NANDI
03680	01C7	3304	MVI A, 04H
03690	01C9	39	CMP C
03700	01CA	3A0702	JZ SUBZI
03710	01C5	3305	MVI A, 05H
03720	01C7	39	CMP C
03730	01D0	3A1402	JZ JANAK
03740	01D3	3306	MVI A, 06H
03750	01D5	39	CMP C
03760	01D6	3A1902	JZ PURI
03770	01D9	331902	JMP PURI
03780	01DC	3AF	KARZ: XRA A
03790	01DD	373	MOV A, E
03800	01DE	335F	ANI 11111100B
03810	01E0	30F	RRC
03820	01E1	30F	RRC
03830	01E2	31E02	JMP GUDDI
03840	01E5	373	KARAM: XRA A
03850	01E6	335F	MOV A, E
03860	01E7	30F	ANI 11110000B
03870	01E9	30F	RRC
03880	01EA	30F	RRC
03890	01EB	30F	RRC
03900	01EC	30F	RRC
03910	01ED	335F	ADI 03FH
03920	01EF	331E02	JMP GUDDI
03930	01F2	373	GANDI: XRA A
03940	01F3	335F	MOV A, E
03950	01F4	335F	ANI 11100000B
03960	01F6	30F	RRC
03970	01F7	30F	RRC
03980	01F8	30F	RRC
03990	01F9	30F	RRC
04000	01FA	30F	RRC
04010	01FB	30F	RRC
04020	01FD	335F	ADI 04EH
04030	0200	331E02	JMP GUDDI
04040	0201	373	NANDI: XRA A
04050	0202	335F	MOV A, E
04060	0204	30F	ANI 11000000B
04070	0205	30F	RRC
04080	0206	30F	RRC
04090	0207	30F	RRC
04100	0208	30F	RRC
04110	0209	30F	RRC
04120	020A	3355	ADI 55H
04130	020C	331E02	JMP GUDDI
04140	020F	3358	SUBZI: MVI A, 58H
04150	0211	331E02	JMP GUDDI
04160	0214	3358	JANAK: MVI A, 058H
04170	0216	331E02	JMP GUDDI
04180	0219	3358	PURI: MVI A, 058H
04190	021B	331E02	JMP GUDDI
04200	021E	30F	GUDDI: MOV A, A
04210	021F	1800	MVI D, 00H
04220	0221	33	PUSH H
04230	0222	211004	LXI H, TANGT
04240	0225	19	DAD D
04250	0226	73	MOV A, M
04260	0227	47	MOV B, A
04270	0228	31	POP B
04280	0229	3A5640	GOA ANLA
04290	022C	3D	DER A
04300	022D	023302	JNZ PATIL

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734402 JMP SOHAM  
 325540 PAUL: STA AMLA  
 346540 LDA VBASE  
 7500 CPT OOH  
 744202 IZ PANAM  
 60 SUR R  
 734302 JMP SOHVC  
 90 PANAM: ADD R  
 325740 SOHVC: STA VANGL  
 23 INX H  
 735301 JMP HATH  
 346540 SOHAM: LDA BASE  
 7500 CPT OOH  
 745502 IZ CAVAL  
 90 SUR R  
 735702 JMP RIVER  
 90 CANAL: ADD R  
 325940 RIVER: STA TANGL

-----  
 CALCULATE IMPEDANCE, COMPARE WITH SET VALUE  
 -----

744202 LHLD SECND  
 7500 XCHG  
 745940 LHLD FIRST  
 7500 MVI R, OH  
 7500 CALL LTQUD  
 7500 REG B = QUOTIENT H-L = REMAINDER  
 7500 REG D-E CONTAINS SECND(DIVISOR)

7500 XRA A  
 7500 MOV A, B  
 7500 RLC  
 7500 RLC  
 7500 RLC  
 7500 ADD B  
 7500 ADD R  
 7500 REG A CONTAINS 10\*QUOTIENT  
 7500 REG PAIR H-L CONTAINS REMAINDER

7500 MOV C, L  
 7500 MOV B, H  
 7500 DAD H  
 7500 DAD H  
 7500 DAD H  
 7500 DAD H  
 7500 DAD H  
 7500 DAD H  
 7500 MOV A, A  
 7500 CHECK WHETHER CONTENTS OF REG H-L  
 7500 IS GREATER THAN CONTENTS OF REG PAIR D-E  
 7500 CONTENTS OF H-L = 10\*REMAINDER

7500 MOV A, L  
 7500 CMP E  
 7500 JC MSUB  
 7500 MOV A, H  
 7500 CMP D  
 7500 JC MONA  
 7500 JMP APPAR  
 7500 MSUB: XRA A  
 7500 MOV A, H  
 7500 OCR A  
 7500 CMP D  
 7500 JC MONA  
 7500 APPAR: CALL LTQUD

-----  
 CALCULATE ANGLE OF IMPEDANCE AND CHECK WHETHER  
 IT LIES WITHIN 0-90 DEGREES  
 -----

7500 MONA: LXI H, VANGL  
 7500 MOV E, B  
 7500 MOV A, B  
 7500 MOV D, A  
 7500 INX H  
 7500 MOV C, H  
 7500 CMP E  
 7500 JC POWER  
 7500 SUB C

05450	0299	23A202	IMP IMPAN
05460	029C	79	POWER: MOV A,C
05470	029D	42	SUB D
05480	029E	17	MOV B,A
05490	029F	38B4	MVT A,084H
05500	02A1	30	SUB B
05510	02A2	065A	IMPAN: MVI B,054H
05520	02A4	83	CMP B
05530	02A5	0AA302	JC STONE
05540	02A8	035F00	IMP ORIGIN
05550			REG A CONTAINS ANGLE OF IMPEDANCE
05560			REG B CONTAINS CALCULATED IMPEDANCE
05570	02A8	57	STONE: MOV D,A
05580	02A7	0641	MVT B,41H
05590	02AE	83	CMP B
05600	02AF	0AR502	JC SALT
05610	02B2	00	SUB B
05620	02B3	03B302	IMP SUGAR
05630	02B6	78	SALT: MOV A,B
05640	02B7	02	SUB D
05650	02B8	03B302	IMP SUGAR
05660	02B9	FE00	SUGAR: CPI 00H
05670	02BD	0AF002	JZ CAMPA
05680			TO CALCULATE ZR**(COS**2)>ZC**
05690	02C0	219004	CALLA: LXI H,COSTA
05700	02C3	42	MOV B,D
05710	02C4	43	MOV C,E
05720	02C5	1600	MVT D,0H
05730	02C7	5F	MOV E,A
05740	02C8	83	ADD E
05750	02C9	57	MOV E,A
05760	02CA	19	DAD D
05770	02CB	72	MOV A,M
05780	02CC	5F	MOV E,A
05790	02CD	23	INX H
05800	02CE	7E	MOV A,M
05810	02CF	57	MOV D,A
05820	02D0	83	XCHG
05830	02D1	226040	SHLD FORTH
05840	02D4	29	DAD H
05850	02D5	29	DAD H
05860	02D6	225E40	SHLD THIRD
05870	02D9	AF	XRA A
05880	02DA	79	MOV A,C
05890	02DB	07	RLC
05900	02DC	07	RLC
05910	02DD	81	ADD C
05920	02DE	06C8	MVI R,0C8H
05930	02E0	007703	CALL MULTI
05940	02E3	FB	XCHG
05950	02E4	2A5E40	LHLD THIRD
05960	02E7	70	MOV A,L
05970	02E8	83	CMP E
05980	02E9	0AF402	JC LIMCA
05990	02EC	7C	MOV A,H
06000	02ED	8A	CMP D
06010	02EE	0A0503	JC ZONE2
06020	02F1	031E04	JMP TRIP1
06030	02F4	7C	LIMCA: MOV A,H
06040	02F5	30	DCR A
06050	02F6	8A	CMP D
06060	02F7	0A0503	JC ZONE2
06070	02FA	031E04	JMP TRIP1
06080	02FD	78	CAMPA: MOV A,E
06090	02FE	FE28	CPI 28H
06100	0300	0A1E04	JC TRIP1
06110	0303	030503	JMP ZONE2
06120			TO CHECK FOR ZONE2 OPERATION
06130			REG PAIR H-L CONTAINS ADDRESS
06140	0306	29	ZONE2: DAD H
06150	0307	226240	SHLD FIFTH
06160	030A	05	PUSH D

0365	37
0366	3F
0367	17
0368	DA7303
036B	1F
036C	F680
036E	2F
036F	3C
0370	C37603

```

+++++
; TO CONVERT THE OFFSET BINARY NUMBER
+++++
DELHI: SEC
CMC
RAL
JC INCCI
RAR
ORI 100000000
CMA
INR A

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JNP: KONGA

0713		
0714		
0715		
0716		
0717		
0718		
0719		
0720		
0721		
0722		
0723	0373	1F
0724	0374	857F
0725	0376	09
0726		
0727		
0728		
0729		
0730		
0731	0377	210000
0732	037A	1503
0733	037C	48
0734	037D	44
0735		
0736	037E	0F
0737	037F	028303
0738	0382	09
0739	0383	15
0740	0384	CA9403
0741	0387	5F
0742	0388	79
0743	0389	37
0744	038A	3F
0745	038B	17
0746	038C	4F
0747	038D	78
0748	038E	17
0749	038F	47
0750	0390	78
0751	0391	C37E03
0752	0394	09
0753		
0754		
0755		
0756	0395	78
0757	0396	1503
0758	0398	1E03
0759	039A	78
0760	039B	FE08
0761	039D	CAAF03
0762	03A0	29
0763	03A1	1C
0764	03A2	7A
0765	03A3	07
0766	03A4	57
0767	03A5	7C
0768	03A6	90
0769	03A7	DAAC03
0770	03AA	14
0771	03AB	67
0772	03AC	239A03
0773	03AF	77
0774	03B0	07
0775	03B1	88
0776	03B2	DAB503
0777	03B5	14
0778	03B6	09
0779		
0780		
0781		
0782		
0783		
0784	03B7	210000
0785	03BA	05
0786	03BB	7A
0787	03BC	2F
0788	03BD	57
0789	03BE	78
0790	03BF	2F
0791	03C0	5F
0792	03C1	13
0793	03C2	3E11
0794	03C4	E5
0795	03C5	19
0796	03C6	02CAD3
0797		
0798		
0799		
0800		
0801		

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TROCI: RAR
ANI 01111111B
KORAR: RET
;+++++
; MULTIPLICATION SUBROUTINE
; MULTIPLIER IN REG A AND MULTIPLICAND IN REG B
; RESULT IN REG PAIR H AND D
;+++++
MULTI: LXI H,0000H
MVI D,0BH
MOV C,D
MOV R,H
; MULTIPLIER IN REG A AND MULTIPLICAND IN B-
CASIJ: RRC
JNC SIGN
DAD B
SIGN: DCR D
JZ ASHTR
MOV E,A
MOV A,C
STC
CMC
RAL
MOV C,A
MOV A,R
RAL
MOV R,A
MOV A,E
JMP CASIJ
ASHTR: RET
;+++++
; DIVISION SUBROUTINE REG D QUOTIENT REG B DIVISOR
;+++++
DIVIS: MOV A,B
MVI D,00H
MVI E,00H
DUSTL: MOV A,E
CPT 0BH
JZ BLADE
DAD H
INR E
MOV A,D
RLC
MOV D,A
MOV A,H
SUB B
JC SOAP
INR D
MOV H,A
SOAP: JMP DUSTL
BLADE: MOV A,H
RLC
CMP B
JC WATER
INR D
WATER: RET
;+++++
; 16 BITS DIVISION SUBROUTINE REG B-C PAIR INITIALLY
; CONTAINS DIVIDEND REG D-E DIVISOR IN END
; REG H-C QUOTIENT, REG H-L CONTAINS REMAINDER
;+++++
DIVISON: LXI H,0000H
PUSH D
MOV A,D
CMA
MOV D,A
MOV A,E
CMA
MOV E,A
INX D
MVI A,17D
MINTDI: PUSH H
DAD B
JNC CRINT

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08020	03C9	83
08030	03CA	81
08040	03CB	85
08050	03CC	79
08060	03CD	17
08070	03CE	4F
08080	03CF	78
08090	03D0	17
08100	03D1	47
08110	03D2	7D
08120	03D3	17
08130	03D4	6F
08140	03D5	7C
08150	03D6	17
08160	03D7	57
08170	03D8	71
08180	03D9	3D
08190	03DA	22C403
08200	03DB	87
08210	03DC	7C
08220	03DD	1F
08230	03DE	57
08240	03DF	7D
08250	03E0	1F
08260	03E1	6F
08270	03E2	01
08280	03E3	29
08290	03E4	7D
08300	03E5	83
08310	03E6	DAF303
08320	03E7	7C
08330	03E8	8A
08340	03E9	DAF803
08350	03EA	7C
08360	03EB	8A
08370	03EC	DAF803
08380	03ED	7C
08390	03EE	8A
08400	03EF	DAF803
08410	03F0	7C
08420	03F1	8A
08430	03F2	DAF803
08440	03F3	7C
08450	03F4	8A
08460	03F5	DAF803
08470	03F6	7C
08480	03F7	8A
08490	03F8	DAF803
08500	03F9	7C
08510	03FA	8A
08520	03FB	DAF803
08530	03FC	7C
08540	03FD	8A
08550	03FE	DAF803
08560	03FF	7C
08570	0400	8A
08580	0401	DAF803
08590	0402	7C
08600	0403	8A
08610	0404	DAF803
08620	0405	7C
08630	0406	8A
08640	0407	DAF803
08650	0408	7C
08660	0409	8A
08670	040A	DAF803
08680	040B	7C
08690	040C	8A
08700	040D	DAF803
08710	040E	7C
08720	040F	8A
08730	0410	DAF803
08740	0411	7C
08750	0412	8A
08760	0413	DAF803
08770	0414	7C
08780	0415	8A
08790	0416	DAF803
08800	0417	7C
08810	0418	8A
08820	0419	DAF803
08830	041A	7C
08840	041B	8A
08850	041C	DAF803
08860	041D	7C
08870	041E	8A
08880	041F	DAF803
08890	0420	7C
08900	0421	8A
08910	0422	DAF803
08920	0423	7C
08930	0424	8A
08940	0425	DAF803
08950	0426	7C
08960	0427	8A
08970	0428	DAF803
08980	0429	7C
08990	042A	8A
09000	042B	DAF803

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XTHL
CHINI: POP 4
PUSH PSA
MOV A,C
RAL
MOV C,A
MOV A,B
RAL
MOV B,A
MOV A,L
RAL
MOV L,A
MOV A,H
RAL
MOV H,A
POP PSW
DCR A
JNZ MINTO
;SHIFT REMAINDER RIGHT & RETURN IN H-L
ORA A
MOV A,H
RAR
MOV H,A
MOV A,L
RAR
MOV L,A
POP D
DAD H
MOV A,L
CMP E
JC LSUB
MOV A,H
CMP D
JC IDNA
JMP SIPP
LSUB: XRA A
MOV A,H
DCR A
CMP D
JC IDNA
SIPP: INX R
IDNA: RET ;REG B=QUOTIENT
;+++++
;TO FIND IMPEDANCE FROM VPEAK AND IPEAK
;+++++
LIQUD: XRA A
MOV A,L
SBR E
MOV L,A
MOV A,H
SBR D
MOV H,A
INR R
XRA A
MOV A,L
CMP E
JC DONE
MOV A,H
CMP D
JC ERASE
JMP LIQUD
DONE: XRA A
MOV A,H
DCR A
CMP D
JC ERASE
JMP LIQUD
ERASE: XRA A
RET ;AS RESULT REG H-L CONTAINS REMAINDER
;+++++
;TRIP SIGNAL
;+++++
TRIP: MVI A,BOM
STA PORTC

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041E	3E80
0420	320260

0423	331204	IMP TRIP1
0426	3320	TRIP2: KVT A, 20H
0428	320260	STA PDRIC
0423	332501	IMP TRIP2
042E	3310	TRIP3: KVT A, 40H
0430	320260	STA PDRIC
0433	332E04	IMP TRIP3
0436	75	NLI
0410		ORG TANGT
0410	02050709	DB 2H, 5H, 7H, 9H, 0BH, 0EH, 10H, 12H, 14H, 16H, 18H
0414	030E1012	
0418	141513	
0413	1A1C101F	DB 1AH, 1CH, 10H, 1FH, 21H, 22H, 24H, 25H, 27H
041F	21222425	
0423	27	
0424	2829232C	DB 28H, 29H, 23H, 2CH, 2DH, 2EH, 2FH, 30H, 31H, 32H
0428	202E2F30	
042C	3132	
042E	33343536	DB 33H, 34H, 35H, 36H, 36H, 37H, 38H, 39H, 39H, 3AH
0432	35373839	
0436	393A	
0438	333B3C3C	DB 3BH, 3BH, 3CH, 3CH, 3DH, 3EH, 3EH, 3EH, 3FH, 3FH
043C	303E3E3E	
0440	3F3F	
0442	40404141	DB 40H, 40H, 41H, 41H, 41H, 42H, 42H, 43H, 43H, 43H
0446	41424243	
044A	4343	
044C	44444445	DB 44H, 44H, 44H, 45H, 45H, 47H, 48H, 49H, 4AH, 4BH
0450	45474849	
0454	4A4B	
0456	434C4C4C	DB 4BH, 4CH, 4CH, 4CH, 4DH, 4EH, 4EH, 4EH, 4FH, 50H
045A	404E4E4E	
045E	4F50	
0460	50515152	DB 50H, 51H, 51H, 52H, 52H, 52H, 53H, 54H, 55H, 55H
0464	52525354	
0468	5555	
046A	56575757	DB 56H, 57H, 57H, 57H, 58H, 58H, 58H
046E	585858	
0490		ORG COSTA
0490	10270327	DB 10H, 27H, 0CH, 27H, 01H, 27H, 0DFH, 26H, 0C4H, 27H
0494	01270F26	
0498	0427	
049A	42267326	DB 0A2H, 26H, 7BH, 26H, 4EH, 26H, 1BH, 26H, 0F2H, 25H
049E	4E261B26	
04A2	5223	
04A4	43255F25	DB 0A3H, 25H, 5FH, 25H, 16H, 25H, 0C6H, 24H, 72H, 24H
04AB	16250624	
04AC	7224	
04AE	1824B923	DB 18H, 24H, 0B9H, 23H, 55H, 23H, 0FCH, 22H, 7EH, 22H
04B2	5523EC22	
04B6	7822	
04B8	05229421	DB 0BH, 22H, 94H, 21H, 19H, 21H, 99H, 20H, 16H, 20H
04BC	19219920	
04CD	1620	
04C2	8E1F031F	DB 8EH, 1FH, 03H, 1FH, 74H, 1EH, 0E1H, 1DH, 4BH, 1DH
04C6	741EE11D	
04CA	4B1D	
04CC	931C1B1C	DB 0B3H, 1CH, 1BH, 1CH, 7AH, 1BH, 0D9H, 1AH, 36H, 1AH
04D0	7A1BD91A	
04D4	3B1A	
04D6	9119EA18	DB 91H, 19H, 0EAH, 18H, 0E1H, 18H, 97H, 17H, 0ECH, 16H
04DA	E1189717	
04DE	E216	
04E0	3F159315	DB 3FH, 16H, 93H, 15H, 0E4H, 14H, 36H, 14H, 87H, 13H
04E4	44143514	
04E8	9713	
04EA	09122B12	DB 009H, 12H, 2BH, 12H, 7DH, 11H, 0D0H, 10H, 23H, 10H
04EE	7041D010	
04F2	2310	
04F4	780FCE0E	DB 78H, 0FH, 0CEH, 0EH, 26H, 0EH, 7EH, 0DH, 0D9H, 0CAH
04F8	260E7E0D	
04FC	030C	
04FE	370C960B	DB 37H, 0CH, 96H, 0BH, 0E0H, 0AH, 0DH, 0AH, 0E0H, 0BH
0502	F80A500A	

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0505 7409
0508 25099C08 DB 2EH,09H,9CH,08H,0DH,08H,82H,07H,0FAH,06H
050C 0008R207
0510 FA05
0512 7A05F605 DB 0DAH,06H,0F6H,05H,7BH,05H,04H,05H,91H,04H
0516 73050405
051A 9104
051C 2304R303 DB 23H,04H,08BH,03H,56H,03H,0F7H,02H,9DH,02H
0520 5503F702
0524 9002
0526 4902FAC1 DB 49H,02H,0FAH,01H,080H,01H,6CH,01H,2CH,01H
052A 80016C01
052E 2C01
0530 F400C200 DB 0F4H,00H,0C2H,00H,94H,00H,06DH,00H,42H,00H
0534 94005000
0538 4C00
053A 30001300 DB 30H,00H,1BH,00H,0CH,00H,03H,00H,00H,00H
053E 0C000300
0542 0000

```

END

NO PROGRAM ERRORS

## SYMBOL TABLE

\* 01

A	0007	AMUA	4056	APPAR	0289	ARMAN	01AB
ASHTR	0394	B	0000	BASE	4065	BLADE	03AF
SDTHM	00A2	C	0001	CAMPA	02FD	CANAL	0256
CABID	031E	CHINT	03CA	COJALA	02C0	CONSTA	0490
CHNPT	6003	D	0002	COTUM	4000	DECRE	0094
DELHT	0365	DERIV	0344	DIVIS	0395	ERASE	0412
DOWNER	00A2	DUSTL	039A	E	0003	FLAKE	0017
FORTH	4062	FINES	0148	FIRST	4059	GHOSE	0098
FORTH	4062	FRESH	0082	GANDI	01F2	HOLCG	005C
GUDOI	021C	H	0004	HARAM	01A1	INTIC	4064
IANGU	4058	IMPAN	02A2	INCR	008C	KARZ	010C
IGNA	037B	JANAK	0214	KARAM	01E5	KUTAB	01AF
KEY	00CB	KISAN	0190	KORAR	0376	LTME	010E
L	0005	LAMB	0021	LIMCA	02F4	M	0006
LIQUD	03FC	LDCK	00C5	LSUB	03F3	NDNA	028C
MANDI	0290	MAXY	00D2	MINTO	03C4	NATH	016E
MSUB	0282	MULTI	0377	NAMAK	0197	PEPSI	0341
ORGIN	006F	PANAM	0242	PAFIL	0233	PORTV	6000
PHULN	0133	PORTC	6002	PORTI	6001	RAJNI	0358
PONER	029C	PSW	0006	PURI	0219	SALT	0028
RANY	035E	RIVER	0257	RST75	003C	SHIFT	0338
SAMPL	00A1	SCROL	031E	SECND	405C	SOAP	03AC
SIGN	0383	STPPU	03F5	SOANG	0243	STONG	03AB
SOHAN	024A	SULO	00D7	SP	0006	TANG	0410
SUBZI	020F	SUGAR	0288	SINOM	0139	TRIP2	0426
THIRD	405E	TRCCI	0373	TRIP1	041E	TRIP3	0426
TRIP3	042E	TUNES	015C	VANGU	4057	VRASE	4056
VDERT	4057	VENKT	0069	YANG	0387	WATER	0388
ZCAL	00E2	ZONE2	0306	ZONE3	0327		

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00180 4000
00190 6000
00200 6001
00210 4020
00220 4022
00230 4024
00240 4026
00250 0500
00260 0520
00270 0540
00280 4027
00290 4028
00300 4029
00310 402A
00320 402B
00330 402C
00340 402D
00350 402E
00360 4030
00370 4032
00380 6002
00390 6003
00400 0000
00410 0000
00420
00430
00440
00450
00460 0003
00470 0005
00480 0008
00490 000A
00500 000D
00510 000F
00520 0012
00530 0015
00540 0017
00550 001A
00560 001B
00570 001E
00580 0021
00590 0024
00600 0027
00610 0028
00620 0029
00630 002C
00640 002F
00650 0030
00660 0031
00670 0034
00680 0037
00690 0038
00700 0039
00710 003A
00720 003B
00730 003C
00740 003D
00750 003E
00760 003F
00770 0042
00780 0044
00790 0047
00800 0048
00810 004A
00820 004B
00830 004E
00840 004F
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31FF42

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REAL TIME MICROPROCESSOR BASED PROGRAMME
FOR QUADILATERAL CHARACTERISTIC DEVELOPED
USING FUNDAMENTAL COMPONENT METHOD TAKING
SAMPLES OVER ONE-HALF POWER CYCLE
-----
/ ASSIGNMENT MEMORY LOCATION FOR VARIABLES
DATUM EQU 4000H ; FOR STORING OF SAMPLES
PORTV EQU 6000H ; PORT 1 FOR VOLTAGE SAMPLE
PORTI EQU 6001H ; PORT 2 FOR CURRENT SAMPLE
FIRST EQU 4020H
SECND EQU 4022H
THIRD EQU 4024H
INTIC EQU 4026H
COSTE EQU 0500H
SINTE EQU 0520H
MITHN EQU 0540H
RESIS EQU 4027H ; STORING RESISTANCE
REACT EQU 4028H ; STORING REACTANCE
VOLR EQU 4029H ; VD COMPONENT OF VOLTAGE
VOLQ EQU 402AH ; VQ COMPONENT OF VOLTAGE
IOLR EQU 402BH ; ID COMPONENT OF CURRENT
IOLQ EQU 402CH ; IQ COMPONENT OF CURRENT
COUNT EQU 402DH
TIGER EQU 402EH
KDMAL EQU 4030H
JAKIN EQU 4032H ; FAULTED SAMPLES
PORTC EQU 6002H ; PORT C OF PPI
CWPPPI EQU 6003H ; CONTROL WORD OF PPI
ORG 0000H
LXI SP,42FFH
;*****
;INITIALISATION OF INPUTPORTS/OUTPUTPORTS AND
;COUNTERS, LOADING OF CONSTANTS
;*****
MVI A,93H
STA CWPPPI
MVI A,00H
STA PORTC
MVI A,00H
STA KDMAL
LXI H,DATUM
MVI C,0CH
FLAKE: LDA PORTC
RAR
JC LAMB
JMP FLAKE
LAMB: LDA PORTV
CALL DELHI
MOV M,A
INX H
LDA PORTI
CALL DELHI
MOV M,A
DCR C
JZ JRESH
JMP FLAKE
NOP
NOP
NOP
NOP
NOP
RST75: PUSH PSW
PUSH H
PUSH D
LDA INTIC
CPI 0H
JZ HOLDG
MOV D,A
MVI A,0CH
SUB D
LXI H,DATUM
MOV E,A
MVI D,0H

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00900
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00990
01000
01010
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01600
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01680
01690
01700
01710
01720
01730
01740
01750
01760
01770
01780
0051 19 DAD D
0052 3A0060 LDA PDRIV
0055 CDEF02 CALL DELHI
0058 77 MOV M,A
0059 C36B00 JMP VENKT
005C 3E0C HLDG: MVI A,0CH
005E 322640 STA INTIC
0061 210040 LXI H,DATUM
0064 3A0060 LDA PDRIV
0067 CDEF02 CALL DELHI
006A 77 MOV M,A
006B 01 VENKT: POP D
006C E1 POP H
006D F1 POP PSW
006E C9 RET
006F 3A2640 ORGIN: LDA INTIC
0072 4F MOV C,A
0073 3E0C MVI A,0CH
0075 91 SUB C
0076 210040 LXI H,DATUM
0079 5F MOV E,A
007A 1600 MVI D,0H
007C 19 DAD D
007D 1E00 MVI E,0H
007F C38900 JMP CHEMS
;-----;
;COLLECTION OF SAMPLES OF VOLTAGE AND CURRENT AND
;CYCLE BY CYCLE COMPARISON OF VOLTAGE SAMPLES AND
;REPLACING THE PREVIOUS BY LATEST SAMPLES OF V & C.
;-----;
0082 1E00 JRESH: MVI E,00H
0084 0E0C FRESH: MVI C,0CH
0086 210040 LXI H,DATUM
0089 3A0260 CHEMS: LDA PDRIC
008C 1F RAR
008D DA9300 JC CSOI
0090 C38900 JMP CHEMS
0093 CDB702 CSOI: CALL SAMP
0096 3E07 MVI A,07H
0098 BB CMP E
0099 CAA700 JZ CALCU
009C AF XRA A
009D 79 MOV A,C
009E FE00 CPI 00H
00A0 CA8400 JZ FRESH
00A3 23 INX H
00A4 C38900 JMP CHEMS
00A7 79 CALCU: MOV A,C
00A8 322640 STA INTIC
00AB 0605 MVI B,06H
00AD BB CMP B
00AE DACE00 JC PENTR
00B1 90 SUB B
00B2 4F MOV C,A
00B3 78 MOV A,B
00B4 91 SUB C
00B5 323040 STA KOMAL
00B8 3E0B MVI A,0BH
00BA 91 SUB C
00BB 0C INR C
00BC 113240 LXI D,JAKIN
00BF CDF903 CALL BNZIR
00C2 3A3040 LDA KOMAL
00C5 4F MOV C,A
00C6 3E00 MVI A,00H
00C8 CDF903 CALL BNZIR
00CB C3DB00 JMP KRODI
00CE 80 PENTR: ADD B
00CF 47 MOV B,A
00D0 3E0B MVI A,0BH
00D2 90 SUB B
00D3 0E07 MVI C,07H
00D5 113240 LXI D,JAKIN
00D8 CDF903 CALL BNZIR

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01790			
01800			
01810			
01820			
01830			
01840			
01850			
01860			
01870			
01880			
01890			
01900			-----
01910			; CALCULATION OF VD
01920	00DB	213240	KRDDI: LXI H, JAKIN
01930	00DE	112D40	LXI D, COUNT
01940	00E1	3E07	MVI A, 07H
01950	00E3	EB	XCHG
01960	00E4	77	MOV M, A
01970	00E5	D5	PUSH D ; FIRST LOCATION WHERE FUNDAMENTAL COMPD STD
01980	00E6	210000	LXI H, 0000H
01990	00E9	222040	SHLD FIRST
02000	00EC	210005	LXI H, COSTE
02010	00EF	CDFF02	CALL SUMMA
02020	00F2	EB	XCHG
02030	00F3	212940	LXI H, VDLR ; PLACE FOR STORING VD
02040	00F6	73	MOV M, E
02050	00F7	D1	POP D
02060			-----
02070			; CALCULATION OF VD
02080			-----
02090	00F8	D5	PUSH D
02100	00F9	212D40	LXI H, COUNT
02110	00FC	3E07	MVI A, 07H
02120	00FE	77	MOV M, A
02130	00FF	210000	LXI H, 0000H
02140	0102	222040	SHLD FIRST
02150	0105	212005	LXI H, SINTE
02160	0108	CDFF02	CALL SUMMA
02170	010B	0650	MVI B, 50H
02180	010D	CD1504	CALL VISON
02190	0110	AF	XRA A
02200	0111	7A	MOV A, D
02210	0112	17	RAL
02220	0113	57	MOV D, A
02230	0114	212A40	LXI H, VDLQ
02240	0117	72	MOV M, D
02250	0118	D1	POP D
02260			-----
02270			; CALCULATION OF ID
02280			-----
02290	0119	13	INX D
02300	011A	D5	PUSH D
02310	011B	212D40	LXI H, COUNT
02320	011E	3E07	MVI A, 07H
02330	0120	77	MOV M, A
02340	0121	210000	LXI H, 0000H
02350	0124	222040	SHLD FIRST
02360	0127	210005	LXI H, COSTE
02370	012A	CDFF02	CALL SUMMA
02380	012D	EB	XCHG
02390	012E	212B40	LXI H, IOLR
02400	0131	73	MOV M, E
02410	0132	D1	POP D
02420			-----
02430			; CALCULATION OF IQ
02440			-----
02450	0133	212D40	LXI H, COUNT
02460	0136	3E07	MVI A, 07H
02470	0138	77	MOV M, A
02480	0139	210000	LXI H, 0000H
02490	013C	222040	SHLD FIRST
02500	013F	212005	LXI H, SINTE
02510	0142	CDFF02	CALL SUMMA
02520	0145	0650	MVI B, 50H
02530	0147	CD1504	CALL VISON
02540	014A	AF	XRA A
02550	014B	7A	MOV A, D
02560	014C	17	RAL
02570	014D	57	MOV D, A
02580	014E	212CA0	LXI H, IOLQ
02590	0151	72	MOV M, D
02600			;
02610			;
02620			;
02630			;
02640			;
02650			;
02660			;

-----  
 $R = VD * ID + VQ * IQ / ID ** 2 + IQ ** 2$   
 -----

0152	212940	LXI H, VOLR
0155	46	MOV B, M
0156	23	INX H
0157	23	INX H
0158	4E	MOV C, M
0159	2B	DCX H
015A	E5	PUSH H
015B	CD9ED3	CALL MULTI ; TO CALCULATE VD*ID
015E	222E40	SHLD TIGER
0161	E1	POP H
0162	46	MOV B, M
0163	23	INX H
0164	23	INX H
0165	4E	MOV C, M
0166	E5	PUSH H
0167	CD9ED3	CALL MULTI ; TO CALCULATE VQ*IQ
016A	E8	XCHG
016B	2A2E40	LHLD TIGER
016E	19	DAD D
016F	222E40	SHLD TIGER ; SUM OF VD*ID+VQ*IQ IS STORED FIRST&FIRST
0172	E1	POP H
0173	46	MOV B, M ; CONTENTS OF IDLO (IQ) MOVED TO REG B
0174	48	MOV C, B
0175	2B	DCX H
0176	E5	PUSH H
0177	CD9ED3	CALL MULTI ; TO CALCULATE (IQ**2)
017A	222240	SHLD SECND
017D	E1	POP H
017E	46	MOV B, M
017F	48	MOV C, B
0180	CD9ED3	CALL MULTI ; TO CALCULATE (ID**2)
0183	E8	XCHG
0184	2A2240	LHLD SECND
0187	19	DAD D
0188	222240	SHLD SECND ; SUM OF (ID**2+IQ**2) IS STORED AT SECND

-----  
 $R = TIGER / SECND$   
 -----

LHLD SECND NOT REQUIRED

018B	EB	XCHG
018C	2A2E40	LHLD TIGER
018F	29	DAD H
0190	29	DAD H
0191	29	DAD H
0192	222040	SHLD FIRST
0195	2A2E40	LHLD TIGER
0198	29	DAD H
0199	4D	MOV C, L
019A	44	MOV B, H
019B	2A2040	LHLD FIRST
019E	09	DAD B
019F	4D	MOV C, L
01A0	44	MOV B, H
01A1	CD8004	CALL LISON
01A4	212740	LXI H, RESIS
01A7	71	MOV M, C

-----  
 $X = VQ * ID - VD * IQ / ID ** 2 + IQ ** 2$   
 -----

01AB	212A40	LXI H, VOLQ
01AB	46	MOV B, M
01AC	23	INX H
01AD	4E	MOV C, M
01AE	23	INX H
01AF	E5	PUSH H

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03570      0180      CD9E03      CALL MULTI ; TO CALCULATE VQ*ID
03580      0183      222440      SHLD THIRD
03590      0186      E1          POP H
03600      0187      46          MOV B,M
03610      0188      2B          DCX H
03620      0189      2B          DCX H
03630      018A      2B          DCX H
03640      018B      4E          MOV C,M
03650      018C      CD9E03      CALL MULTI ; TO CALCULATE VD*IQ
03660      018F      CD7704      CALL IWCCM
03670      01C2      EB          XCHG
03680      01C3      2A2440      LHLD THIRD
03690      01C6      19          DAD D
03700      01C7      222440      SHLD THIRD
03710
03720      ;-----
03730      ; TO CALCULATE X = THIRD/SECND
03740      ;-----
03750      ; LHLD THIRD NOT REQUIRED
03760
03770      01CA      29          DAD H
03780      01CB      29          DAD H
03790      01CC      29          DAD H
03800      01CD      222040      SHLD FIRST
03810      01D0      2A2440      LHLD THIRD
03820      01D3      29          DAD H
03830      01D4      4D          MOV C,L
03840      01D5      44          MOV B,H
03850      01D6      2A2040      LHLD FIRST
03860      01D9      09          DAD B
03870      01DA      4D          MOV C,L
03880      01DB      44          MOV B,H
03890      01DC      2A2240      LHLD SECND
03900      01DF      EB          XCHG
03910      01E0      CD8004      CALL LISON
03920      01E3      212840      LXI H,REACT
03930      01E6      71          MOV M,C
03940
03950      ;-----
03960      ; RELAY LOGIC FOR QUADRILATERAL CHARACTERISTIC
03970      ; TO CHECK WHETHER R > 0 OR NOT
03980      ; TO CHECK WHETHER X > 0 OR NOT
03990      ; TO CHECK WHETHER R < R3 OR NOT
04000      ; TO CHECK WHETHER R < R2
04010      ; TO CHECK WHETHER R > R1 OR NOT
04020      ; TO CHECK WHETHER K4 > K2 K4=X/R-R2, K2=X1/R3-R2
04030      ; TO CHECK WHETHER K3 < K1 K3=X/R K1=X1/R1
04040      ; TO CHECK FOR ZONE1 ZONE2 ZONE3
04050      ;-----
04060      04130      01E7      AF          XRA A
04070      04140      01E8      212740      LXI H,RESIS
04080      04150      01EB      46          MOV B,M
04090      04160      01EC      23          INX H
04100      04170      01ED      4E          MOV C,M ; REG B=RESISTANCE, REG C=REACTANCE
04110      ; TO CHECK WHETHER R > 0 OR NOT
04120      04180      01EE      78          MOV A,B
04130      04190      01EF      B7          DRA A
04140      04200      01F0      FA6F00      JM ORGIN
04150      ; TO CHECK WHETHER X > 0 OR NOT
04160      04220      01F3      79          MOV A,C
04170      04240      01F4      B7          DRA A
04180      04250      01F5      FA6F00      JM ORGIN
04190      ; TO CHECK WHETHER X < X1
04200      04270      01FB      161E      MVI D,1EH
04210      04280      01FA      BA          CMP D
04220      04290      01FB      D23B02      JNC ZONE2
04230      ; TO CHECK WHETHER R < R3 OR NOT
04240      04310      01FE      1611      MVI D,11H
04250      04320      0200      78          MOV A,B
04260      04330      0201      BA          CMP D
04270      04340      0202      D23B02      JNC ZONE2
04280      ; TO CHECK WHETHER R < R2
04290      04360      0205      160E      MVI D,0EH
04300      04370      0207      BA          CMP D
04310      04380      0208      D21402      JNC ARMAN
04320      ; TO CHECK WHETHER R > R1
04330      04400      020B      1603      MVI D,03H
04340

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04460 020D BA CMP D
04470 020E DA2702 JC APPU
04480 0211 C3C504 JMP TRIP1
04490 ; TO CHECK WHETHER K4 > K2 AND CALCULATION OF K4
04500 0214 AF ARMAN: XRA A
04510 0215 160E MVI D,0EH
04520 0217 78 MOV A,B
04530 0218 92 SUB D
04540 0219 47 MOV B,A
04550 021A CD5304 CALL DIVIS
04560 021D 7A MOV A,D
04570 021E 160A MVI D,0AH
04580 0220 BA CMP D
04590 0221 DA6F00 JC ORGIN
04700 0224 C3C504 JMP TRIP1
04710 ; TO CHECK WHETHER K3 < K1
04720 0227 AF APPU: XRA A
04730 0228 CD5304 CALL DIVIS
04740 022B 7A MOV A,D
04750 022C 160A MVI D,0AH
04760 022E BA CMP D
04770 022F D23502 JNC LRESH
04780 0232 C3C504 JMP TRIP1
04790 0235 CAC504 LRESH: JZ TRIP1
04800 0238 C38400 JMP FRESH
04810 ; ++++++
04820 ; TO CHECK FOR ZONE2 OPERATION
04830 ; ++++++
04840 ; TO CHECK WHETHER X < X1
04850 023B 163C ZONE2: MVI D,3CH
04860 023D 79 MOV A,C
04870 023E BA CMP D
04880 023F D27902 JNC ZONE3
04890 ; TO CHECK WHETHER R<R3 OR NOT
04900 0242 1614 MVI D,14H
04910 0244 78 MOV A,B
04920 0245 BA CMP D
04930 0246 D27902 JNC ZONE3
04940 ; TO CHECK WHETHER R<R2 OR NOT
04950 0249 160E MVI D,0EH
04960 024B BA CMP D
04970 024C D25802 JNC ZSMPP
04980 ; TO CHECK WHETHER R>R1
04990 024F 1606 MVI D,06H
05000 0251 BA CMP D
05010 0252 DA6B02 JC QSTRI
05020 0255 C3CD04 JMP TRIP2
05030 ; TO CHECK WHETHER K4>K2 AND CALCULATION OF K4
05040 0258 AF ZSMPP: XRA A
05050 0259 160E MVI D,0EH
05060 025B 78 MOV A,B
05070 025C 92 SUB D
05080 025D 47 MOV B,A
05090 025E CD5304 CALL DIVIS
05100 0261 7A MOV A,D
05110 0262 160A MVI D,0AH
05120 0264 BA CMP D
05130 0265 DA6F00 JC ORGIN
05140 0268 C3CD04 JMP TRIP2
05150 ; TO CHECK WHETHER K3<K1
05160 026B AF QSTRI: XRA A
05170 026C CD5304 CALL DIVIS
05180 026F 7A MOV A,D
05190 0270 160A MVI D,0AH
05200 0272 BA CMP D
05210 0273 D26F00 JNC ORGIN
05220 0276 C3CD04 JMP TRIP2
05230 ; ++++++
05240 ; TO CHECK FOR ZONE3 OPERATION
05250 ; ++++++
05260 ; TO CHECK WHETHER X < X1
05270 0279 165A ZONE3: MVI D,5AH
05280 027B 79 MOV A,C

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05350
05360
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05420
05430
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05450
027C BA CMP D
05460 027D D26F00 JNC ORGIN
; TO CHECK WHETHER R<R3 OR NOT
05470
05480 0280 1617 MVI D,17H
05490 0282 78 MOV A,B
05500 0283 BA CMP D
05510 0284 D26F00 JNC ORGIN
; TO CHECK WHETHER R<R2 OR NOT
05520
05530 0287 160E MVI D,0EH
05540 0289 BA CMP D
05550 028A D29502 JNC PSMVM
; TO CHECK WHETHER R>R1
05560
05570 028D 1609 MVI D,09H
05580 028F BA CMP D
05590 0290 DAA902 JC MALOP
05600 0293 C3D504 JMP TRIP3
; TO CHECK WHETHER K4>K2 AND CALCULATION OF K4
05610
05620 0296 AF PSMVM: XRA A
05630 0297 160E MVI D,0EH
05640 0299 78 MOV A,B
05650 029A 92 SUB D
05660 029B 47 MOV B,A
05670 029C CD5304 CALL DIVIS
05680 029F 7A MOV A,D
05690 02A0 160A MVI D,0AH
05700 02A2 BA CMP D
05710 02A3 DA6F00 JC ORGIN
05720 02A6 C3D504 JMP TRIP3
; TO CHECK WHETHER K3<K1
05730
05740 02A9 AF MALOP: XRA A
05750 02AA CD5304 CALL DIVIS
05760 02AD 7A MOV A,D
05770 02AE 160A MVI D,0AH
05780 02B0 BA CMP D
05790 02B1 D26F00 JNC ORGIN
05800 02B4 C3D504 JMP TRIP3
;-----
; SUBROUTINES
;-----
05810
05820
05830
05840 02B7 46 SAMP : MOV B,M
05850 02B8 3AD060 LDA PORTV
05860 02BB CDEF02 CALL DELHI
05870 02BE 77 MOV M,A
05880 02BF 23 INX H
05890 02C0 3AD160 LDA PORTI
05900 02C3 CDEF02 CALL DELHI
05910 02C6 77 MOV M,A
05920 02C7 2B DCX H
05930
05940 02C8 78 ; TO COMPARE THE VOLTAGE SAMPLES
05950 02C9 56 MOV A,B
05960 02CA BA MOV D,M
05970 02CB DAD102 CMP D
05980 02CE C3D302 JC LOCK
05990 02D1 7A JMP KEY
06000 02D2 50 LOCK : MOV A,D
06010 02D3 92 MOV D,B
06020 02D4 1605 KEY : SUB D
06030 02D6 BA MVI D,05H
06040 02D7 DADD02 CMP D
06050 02DA C3EB02 JC MAXY
06060 02DD AF JMP SOLO
06070 02DE 23 MAXY : XRA A
06080 02DF 3E00 INX H
06090 02E1 8B MVI A,00H
06100 02E2 CAE602 CMP E
06110 02E5 1D JZ GH0ST
06120 02E6 AF DCR E
06130 02E7 0D GH0ST: XRA A
06140 02E8 CBEE02 DCR C
06150 02EB 1C JMP JULLD
06160 02EC 23 SOLO : INR E
06170 02ED 0D INX H
06180 02EE C9 DCR C
06190
06200
06210
06220
06230

```

06240		
06250		
06260		
06270		
06280		
06290		
06300		
06310		
06320		
06330		
06340		
06350		
06360		
06370	02EF	37
06380	02F0	3F
06390	02F1	17
06400	02F2	DAFB02
06410	02F5	1F
06420	02F6	F680
06430	02F8	C3FE02
06440	02FB	1F
06450	02FC	E67F
06460	02FE	C9
06470		
06480		
06490		
06500	02FF	AF
06510	0300	46
06520	0301	23
06530	0302	EB
06540	0303	4E
06550	0304	23
06560	0305	23
06570	0306	EB
06580	0307	E5
06590	0308	D5
06600	0309	78
06610	030A	B7
06620	030B	F21003
06630	030E	2F
06640	030F	3C
06650	0310	1603
06660	0312	BA
06670	0313	DA1D03
06680	0316	AF
06690	0317	CD9ED3
06700	031A	C32003
06710	031D	CD5A03
06720	0320	EB
06730	0321	2A2040
06740	0324	19
06750	0325	222040
06760	0328	212D40
06770	032B	7E
06780	032C	3D
06790	032D	C23303
06800	0330	C38903
06810	0333	77
06820	0334	D1
06830	0335	E1
06840	0336	C3FF02
06850	0339	D1
06860	033A	E1
06870	033B	2A2040
06880	033E	7C
06890	033F	B7
06900	0340	FAACD3
06910	0343	7C
06920	0344	1F
06930	0345	67
06940	0346	7D
06950	0347	1F
06960	0348	6F
06970	0349	C35903
06980	034C	CD7704
06990	034F	AF
07000	0350	7C
07010	0351	1F
07020	0352	67
07030	0353	7D
07040	0354	1F
07050	0355	6F
07060	0356	CD7704
07070	0359	C9

```

;+++++
;TO CONVRT THE OFFSET BINARY NUMBER
;+++++

```

```

DELHI: STC
CMC
RAL
JC RAJNI
RAR
ORI 10000000B
JMP KORAR
RAJNI: RAR
ANI 01111111B
KORAR: RET

```

```

;-----
; TO CALCULATE THE SUM OVER DATA WINDOW
;-----

```

```

SUMMA: XRA A
MOV B,M
INX H
XCHG
MOV C,M
INX H
INX H
XCHG
PUSH H
PUSH D
MOV A,B
ORA A
JP MONDI
CMA
INR A
MONDI: MVI D,03H
CMP D
JC SURII
XRA A
CALL MULTI
JMP LURID
SURII: CALL COSMU
LURID: XCHG
LHLD FIRST
DAD D
SHLD FIRST
LXI H,COUNT
MOV A,M
DCR A
JNZ PATIL
JMP KIRTI
PATIL: MOV M,A
POP D
POP H
JMP SUMMA
KIRTI: POP D
POP H
LHLD FIRST
MOV A,H
ORA A
JM BINDU
MOV A,H
RAR
MOV H,A
MOV A,L
RAR
MOV L,A
JMP RDBUR
BINDU: CALL TWOCH
XRA A
MOV A,H
RAR
MOV H,A
MOV A,L
RAR
MOV L,A
CALL TWOCH
RDBUR: RET

```

039E	C5
039F	78
03A0	E680
03A2	FED0
03A4	CAAB03
03A7	78
03A8	2F
03A9	3C
03AA	47
03AB	79
03AC	E680
03AE	FED0
03B0	CAB703
03B3	79
03B4	2F
03B5	3C
03B6	4F
03B7	78
03B8	FED0
03BA	CAF403

```

;+++++
;TO CALCULATE THE PRODUCT OF COSINE TERMS
;+++++
CDSMU: PUSH B ;REG B =CONSTANT REG C =SAMPLE VALUE
MOV A,B
DRA A
JP DVOS
CMA
INR A
MOV B,A
DVOS: MOV A,C
DRA A
JP VALM
CMA
INR A
MOV C,A
VALM: MOV A,B
CPI 00H
JZ SINGM
MOV A,C
CPI 00H
JZ SINGM
LXI H,0000H
MVI D,00H
MOV E,C
ARADN: DAD D
DCR B
JZ MANJI
JMP ARADN
MANJI: POP B
XRA A
MOV A,B
XRA C
JM GUDWR
JMP NANKA
GUDWR: MOV A,L
CMA
MOV L,A
MOV A,H
CMA
MOV H,A
INX H
JMP NANKA
SINGM: POP B
LXI H,0000H
NANKA: RET
;-----
; MULTIPLICATION REG B=CONSTANT REG C=SAMPLE
;-----
MULTI: PUSH B
MOV A,B
ANI 10000000B
CPI 00H
JZ GARG
MOV A,B
CMA
INR A
MOV B,A
GARG: MOV A,C
ANI 10000000B
CPI 00H
JZ ABHA
MOV A,C
CMA
INR A
MOV C,A
ABHA: MOV A,B
CPI 00H
JZ RITA

```

```

08020 03BD 79 MOV A,C
08030 03BE FE00 CPI 00H
08040 03C0 CAF403 JZ RIFA
08050 03C3 78 MOV A,B;REGA=MULTIPLIER REG C=MULTIPLICANT RES LV H-.
08060 03C4 210000 LXI H,00H
08070 03C7 1608 MVI D,08H
08080 03C9 44 MOV B,H
08090 03CA 0F CASIO: RRC
08100 03CB 02CF03 JNC SIGN
08110 03CE 09 DAD B
08120 03CF 15 SIGN: DCR D
08130 03D0 CAE003 JZ ASHTR
08140 03D3 5F MOV E,A
08150 03D4 79 MOV A,C
08160 03D5 37 SIC
08170 03D6 3F CMC
08180 03D7 17 RAL
08190 03D8 4F MOV C,A
08200 03D9 78 MOV A,B
08210 03DA 17 RAL
08220 03DB 47 MOV B,A
08230 03DC 78 MOV A,E
08240 03DD C3CA03 JMP CASIO
08250 03E0 C1 ASHTR: POP B
08260 03E1 AF XRA A
08270 03E2 78 MOV A,B
08280 03E3 A9 XRA C
08290 03E4 FAE403 JM KUNAT
08300 03E7 C3F803 JMP ARABN
08310 03EA 7D KUNAT: MOV A,L
08320 03EB 2F CMA
08330 03EC 6F MOV L,A
08340 03ED 7C MOV A,H
08350 03EE 2F CMA
08360 03EF 67 MOV H,A
08370 03F0 23 INX H
08380 03F1 C3F803 JMP ARABN
08390 03F4 C1 RITA: POP B
08400 03F5 210000 LXI H,0000H
08410 03F8 C9 ARABN: RET
;+++++
;TO DERIVE SINGLE PHASE RELAYING QUANTITIES
;+++++
08420 03F9 214005 BNZIR: LXI H, WITHN
08430 03FC 85 ADD L
08440 03FD 6F MOV L,A
08450 03FE 7E MOV A,M
08460 03FF 210040 LXI H,DATUM
08470 0402 85 ADD L
08480 0403 6F MOV L,A
08490 0404 7E ROMA: MOV A,M
08500 0405 EB XCHG
08510 0406 77 MOV M,A
08520 0407 23 INX H
08530 0408 EB XCHG
08540 0409 23 INX H
08550 040A 7E MOV A,M
08560 040B EB XCHG
08570 040C 77 MOV M,A
08580 040D 23 INX H
08590 040E EB XCHG
08600 040F 23 INX H
08610 0410 0D DCR C
08620 0411 C20404 JNZ ROMA
08630 0414 C9 RET
;+++++
;16BIT DIVISON SUBROUTINE
;+++++
08640 0415 E5 VISON: PUSH H
08650 0416 7C MOV A,H
08660 0417 E680 ANI 10000000B
08670 0419 FE00 CPI 00H
08680 041B CA2504 JZ RINKU
08690 041E 7C MOV A,H

```

```

08910 041F 2F CMA
08920 0420 67 MOV H,A
08930 0421 7D MOV A,I
08940 0422 2F CMA
08950 0423 6F MOV L,A
08960 0424 23 TNX H
08970 0425 1600 RINKU: MVI D,00H
08980 0427 1E00 MVI E,00H
08990 0429 7B CHINT: MOV A,E
09000 042A FE08 CPI 08H
09010 042C CA3E04 JZ MINTO
09020 042F 29 DAD H
09030 0430 1C INR E
09040 0431 7A MOV A,D
09050 0432 07 RLC
09060 0433 57 MOV D,A
09070 0434 7C MOV A,H
09080 0435 90 SUB B
09090 0436 DA3B04 JC BAWA
09100 0439 14 INR D
09110 043A 67 MOV H,A
09120 043B C32904 BAWA: JMP CHINT
09130 043E 7C MINTO: MOV A,H
09140 043F 07 RLC
09150 0440 B8 CMP B
09160 0441 DA4504 JC BANTI
09170 0444 14 INR D
09180 0445 E1 BANTI: POP H
09190 0446 7C MOV A,H
09200 0447 E680 ANI 10000000B
09210 0449 FE00 CPI 00H
09220 044B CA5204 JZ NEEL
09230 044E 7A MOV A,D
09240 044F 2F CMA
09250 0450 57 MOV D,A
09260 0451 14 INR D
09270 0452 C9 NEEL: RET

```

```

;-----;
; DIVISON
;-----;

```

```

09410 0453 AF DIVIS: XRA A
09420 0454 78 MOV A,B
09430 0455 69 MOV L,C
09440 0456 2600 MVI H,00H
09450 0458 54 MOV D,H
09460 0459 5C MOV E,H
09470 045A 7B DUSTL: MOV A,E
09480 045B FE08 CPI 08H
09490 045D CA6F04 JZ BLADE
09500 0460 29 DAD H
09510 0461 1C INR E
09520 0462 7A MOV A,D
09530 0463 07 RLC
09540 0464 57 MOV D,A
09550 0465 7C MOV A,H
09560 0466 90 SUB B
09570 0467 DA6C04 JC SOAP
09580 046A 14 INR D
09590 046B 67 MOV H,A
09600 046C C35A04 SOAP: JMP DUSTL
09610 046F 7C BLADE: MOV A,H
09620 0470 07 RLC
09630 0471 B8 CMP B
09640 0472 DA7604 JC WATER
09650 0475 14 INR D
09660 0476 C9 WATER: RET

```

```

;-----;
; TWOCM
;-----;

```

```

09700 0477 AF TWOCM: XRA A
09710 0478 7D MOV A,L
09720 0479 2F CMA
09730 047A 6F MOV L,A
09740 047B 7C MOV A,H

```

```

047C 2F CMA
047D 67 MOV H,A
047E 23 INX H
047F C9 RET

```

```

0480 210000

```

```

0483 05

```

```

0484 7A

```

```

0485 2F

```

```

0486 57

```

```

0487 7B

```

```

0488 2F

```

```

0489 5F

```

```

048A 13

```

```

048B 3E11

```

```

048D E5

```

```

048E 19

```

```

048F 029304

```

```

0492 E3

```

```

0493 E1

```

```

0494 F5

```

```

0495 79

```

```

0496 17

```

```

0497 4F

```

```

0498 78

```

```

0499 17

```

```

049A 47

```

```

049B 7D

```

```

049C 17

```

```

049D 6F

```

```

049E 7C

```

```

049F 17

```

```

04A0 67

```

```

04A1 F1

```

```

04A2 3D

```

```

04A3 C28D04

```

```

04A6 B7

```

```

04A7 7C

```

```

04A8 1F

```

```

04A9 67

```

```

04AA 7D

```

```

04AB 1F

```

```

04AC 6F

```

```

04AD 29

```

```

04AE D1

```

```

04AF 7D

```

```

04B0 BB

```

```

04B1 DABCD4

```

```

04B4 7C

```

```

04B5 BA

```

```

04B6 DAC404

```

```

04B9 C3C304

```

```

04BC AF

```

```

04BD 7C

```

```

04BE 3D

```

```

04BF BA

```

```

04C0 DAC404

```

```

04C3 03

```

```

04C4 C9

```

```

CMA
MOV H,A
INX H
RET

```

```

;=====
;16 BITS DIVISON SUBROUTINE. REG B-C PAIR INITIALLY DIV
;REG PAIR D-E CONTAINS DIVISOR AND IN THE END REG B-
;QUOTIENT, REG D-E CONTAINS REMAINDER
;=====

```

```

LISON: LXI H,0000H

```

```

PUSH D

```

```

MOV A,D

```

```

CMA

```

```

MOV D,A

```

```

MOV A,E

```

```

CMA

```

```

MOV E,A

```

```

INX D

```

```

MVI A,17D

```

```

LINTO: PUSH H

```

```

DAD D

```

```

JNC RHINT

```

```

XTHL

```

```

RHINT: POP H

```

```

PUSH PSW

```

```

MOV A,C

```

```

RAL

```

```

MOV C,A

```

```

MOV A,R

```

```

RAL

```

```

MOV B,A

```

```

MOV A,L

```

```

RAL

```

```

MOV L,A

```

```

MOV A,H

```

```

RAL

```

```

MOV H,A

```

```

POP PSW

```

```

DCR A

```

```

JNZ LINTO

```

```

;SHIFT REMAINDER RIGHT & RETURN IN H-L

```

```

ORA A

```

```

MOV A,H

```

```

RAR

```

```

MOV H,A

```

```

MOV A,L

```

```

RAR

```

```

MOV L,A

```

```

DAD H

```

```

POP D

```

```

MOV A,L

```

```

CMP E

```

```

JC MSUB

```

```

MOV A,H

```

```

CMP D

```

```

JC MONA

```

```

JMP DIPPU

```

```

MSUB: XRA A

```

```

MOV A,H

```

```

DCR A

```

```

CMP D

```

```

JC MONA

```

```

DIPPU: INX B

```

```

MONA: RET ; REG B-C=QUOTIENT

```

```

;-----

```

```

;TRIP

```

```

;-----

```

```

;TRIP1:MVI A,80H

```

```

STA PORTC

```

```

JMP TRIP1

```

```

04C5 3E80

```

```

04C7 320260

```

```

04CA C3C504

```

10690  
10700  
10710  
10720  
10730  
10740  
10750  
10760  
10770  
10780  
10790  
10800  
10810  
10820  
10830  
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10870  
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10890  
10900  
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10980  
10990  
11000  
11010  
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11090  
11100  
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11200  
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11260  
11270  
11280  
11290  
11300  
11310  
11320  
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11360  
11370  
11380  
11390  
11400  
11410  
11420  
11430  
11440  
11450  
11460

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```

04CD 3E20 TRIP2: MVT A,20H
04CF 320260 STA PJRTIC
04D2 C3CD04 JMP TRIP2
04D5 3E40 TRIP3: MVT A,40H
04D7 320260 STA PJRTIC
04DA C3D504 JMP TRIP3
04DD 76 HLT
0520 ORG SINTE
0520 00232300 DB 00H,23H,23H,00H,-23H,-23H
0524 000D00
0500 ORG COSTE
0500 FFFF0102 DB -1H,-1H,1H,2H,1H,-1H,-1H
0504 01FFFF
0540 ORG MITHN
0540 00020406 DB 00H,02H,04H,06H,08H,0AH,0CH,0EH,10H,12H,14H,16H
0544 080A0C0E
0548 10121416

END
NO PROGRAM ERRORS

```

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# SYMBOL TABLE

\* 01

A	0007	ABHA	03B7	APPU	0227	ARABN	03F8
ARADN	037D	ARMAN	0214	ASHTR	03E0	B	0000
BANII	0445	BAWA	043B	BINDU	034C	BLADE	046F
BNZIR	03F9	C	0001	CALCU	00A7	CASIO	03CA
CHEMS	0089	CHINT	0429	COSMU	035A	COSTE	0500
COUNT	402D	CSOI	0093	CNPPI	6003	D	0002
DATUM	4000	DELHI	02EF	DIPPU	04CB	DIVIS	0453
DUSTL	045A	DVDS	0363	E	0003	FIRST	4020
FLAKE	0017	FRESH	0084	GARG	03AB	GHOST	02E6
GUDWR	038F	H	0004	HJLOG	005C	INTIC	4026
IDLQ	402C	IDLR	402B	JAKIN	4032	JRESH	0082
JULLD	02EE	KEY	02D3	KIRTI	0339	KOMAL	4030
KORAR	02FE	KRODI	00DB	KUNAT	03EA	L	0005
LAMB	0021	LINTD	048D	LISON	0480	LOCK	02D1
LRESH	0235	LURID	0320	M	0006	MALCP	02A9
MANJI	0385	MAXY	02DD	MINTD	043E	MITHN	0540
MONA	04C4	MONDI	0310	MSUB	04BC	MULTI	039E
NANKA	039D	NEEL	0452	ORGIN	006F	PATIL	0333
PENTR	00CE	PORTC	6002	PJRTI	6001	PJRTV	6000
PSMMM	0296	PSW	0006	QSTRI	026B	RAJNI	02FB
RDBUR	0359	REACT	4028	RESIS	4027	RHINT	0493
RINKU	0425	RITA	03F4	RJMA	0404	RST75	003C *
SAMP	02B7	SECND	4022	SIGN	03CF	SINGM	0399
SINTE	0520	SOAP	046C	SOLO	02EB	SP	0006
SUMMA	02FF	SURII	031D	THIRD	4024	TIGER	402E
TRIP1	04C5	TRIP2	04CD	TRIP3	04D6	TWOCM	0477
VALM	036B	VENKT	006B	VISON	0415	VOLA	402A
VOLR	4029	WATER	0476	ZJNE2	023B	ZONEB	0279
ZSMPP	0258						